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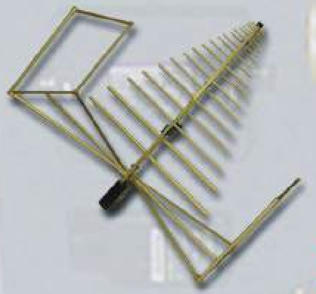

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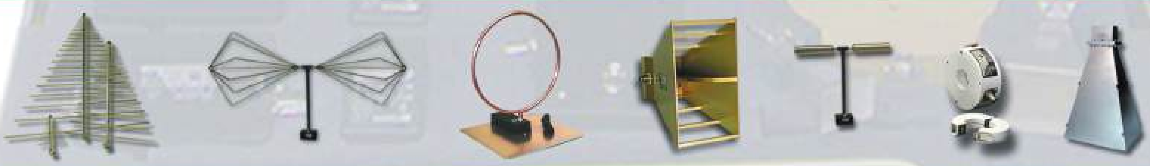

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EDITORIAL:
THE IMPORTANCE OF EMC EDUCATION

Dean Landers
E3 Engineer I landers.dean@gmail.com

As most readers of Interference Technology know, our industry is aging, and the youth movement is due to catch up at some point. Until that happens, we rely on the tribal knowledge of a few select experts to guide the youth along the way.

But if I take a step back and look, I ask the question, "Who guided those who came before me?" And the answer is usually nobody. The likes of Henry Ott and Don Heirman are no longer with us, and many others are approaching retirement or are already there.

Thus, as an industry, we need to come to grips with taking our industry into the future with the younger generation via lab experience and education in EMI/EMC as a discipline. At the risk of sounding like a curmudgeon: Back in my day, there wasn't much in the way of educational programs at universities on EMI/EMC, unless I was completely oblivious to it. Today, you can find programs and professors around the country involved in EMC education and furthering the science, which is dearly needed.

With a changing economic landscape and an aging core of members approaching retirement, the time is now (or hopefully not past) to educate and train younger engineers and technicians on EMC. This includes the technical writing aspect of procedures and reports, specification development, understanding requirements and their intent, and performing testing. In the world of military and commercial aviation testing, now, more than ever, education and training for MIL-STD-461 and RTCA/DO-160 is needed by the manufacturers as product development continues to ramp up with a rolling landscape of engineering in these areas.

And yes, a lot can be learned by searching the web and reading, but the execution of the tasks is a bit of a craft. Also, the move towards digital engineering has sparked the need for MODSIM execution for understanding the behavior of equipment in certain environments (radar, lightning, wireless coexistence, etc.), and these answers cannot be found on Google. Not easily, anyway.

So, to the young people out there who may have engineering degrees but little direction or employment opportunities, look into a career in EMC. It might just be your ticket into a future in a niche industry. I implore those looking for careers in this area to start with articles in this publication, as they aim to educate, train, and instruct those within our collective to increase knowledge and awareness. Also, find meetings in your local area to network, discuss, and learn more about who is involved in our subject matter.

EMC AND RELIABILITY IN FLEX PCB CABLES VS. CABLE ASSEMBLIES

Zachariah Peterson
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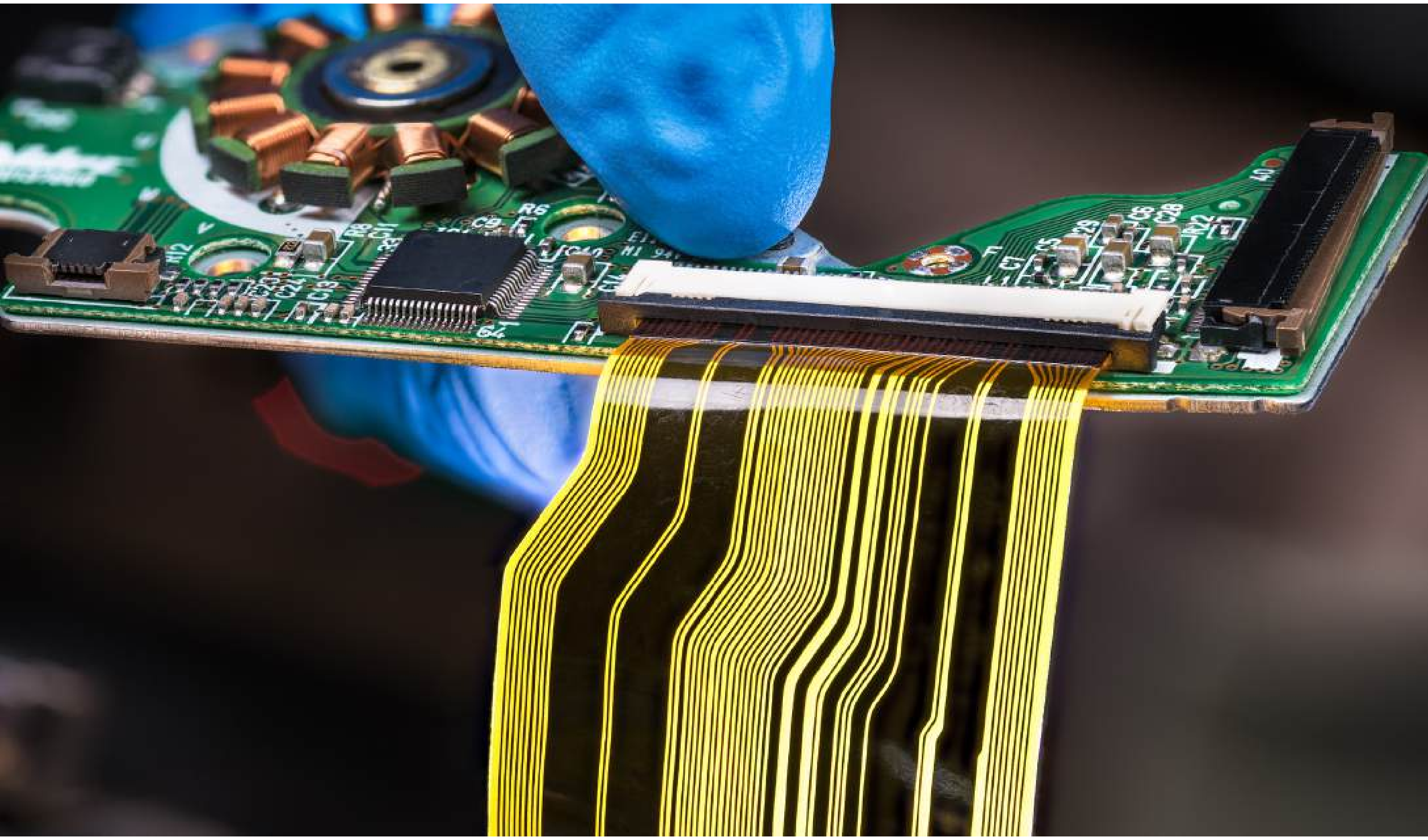


In military and aerospace systems, interconnect failure isn't just an inconvenience; it can mean mission failure, equipment loss worth millions of dollars, or in the worst case, loss of life. Every connection between circuit boards represents a potential point of failure that must withstand extreme environmental conditions while maintaining signal integrity and EMC in increasingly compact systems. Traditional cabling solutions face routing and mounting challenges in modern defense applications where devices are placed in smaller packages, with the most recent examples being miniaturized UAV flight control systems, densely packed phased array radar modules, and wearables for personnel on the battlefield.

Flexible printed circuit (FPC) interconnects can be designed as custom components that can replace a much larger cable assembly or wiring harness. The choice between FPCs versus custom cabling creates trade-offs that directly impact system reliability, electromagnetic performance, and mission success in defense applications. Understanding these trade-offs is essential for engineers developing the next generation of military and aerospace electronic systems.

MIL-AERO INTERCONNECT DESIGN CHALLENGES

Military and aerospace electronic systems operate in environments that would destroy most commercial electronics. Temperature extremes ranging from -55°C in high-altitude reconnaissance missions to +125°C in engine bay applications create thermal cycling stresses that can cause solder joint failure and material degradation. Humidity, salt spray, and chemical exposure in naval applications add corrosion challenges, while radiation exposure in space-based systems can degrade insulation materials and cause single-event upsets in sensitive circuits.

- **Bend radius control:** Minimum 6x cable thickness to prevent copper fatigue
- **Vibration resistance:** Must withstand 0.01-2 kHz per MIL-STD-810
- **Current density:** Limit to 1000 A/in² for flex circuits vs. 3000 A/in² for wire
- **Impedance tolerance:** ±10% maximum variation across temperature range
- **Shielding effectiveness:** >40 dB required for sensitive RF applications

Environmental Parameter	Commercial Spec	Mil-Aero Requirement	Design Impact
Operating Temperature	0°C to +70°C	-55°C to +125°C	Requires polyimide substrates
Shock Resistance	10G	100G+	Reinforced connector interfaces
EMI Shielding	20 dB typical	>40 dB required	Hatched ground planes needed

Mechanical stresses present equally demanding challenges. Aircraft and missile systems must survive shock loads and continuous vibration across broad frequency spectrums as defined in MIL-STD-810. These conditions can cause wire fatigue, connector loosening, and intermittent connections that are difficult to diagnose and potentially catastrophic in operation. Supply chain security requirements further limit component choices, requiring ITAR-compliant fabrication vendors and component sources.

EMI/EMC DESIGN COMPARISON

EMC presents one of the most challenging aspects of interconnect design in military and aerospace systems, where standard commercial approaches often fall short of meeting stringent defense requirements. The unique construction of flexible printed circuit cables requires careful consideration of hatched ground plane design to achieve adequate EMI shielding while maintaining mechanical flexibility.

- **Hatch opening size:** Often taken to be λ/4 to λ/20 at highest frequency of concern
- **Pattern offset:** Stagger openings between layers for improved shielding effectiveness
- **Edge rate limitation:** Sub-nanosecond signals may exceed hatched plane capabilities

Interconnect Type	Shielding Effectiveness	Flexibility	Power Handling	Best Application
Off-the-shelf FPC	20-30 dB	High (single axis)	<2A per trace	Low power, digital
Custom hatched flex	35-45 dB	Good (dynamic or static bend)	<5A per trace	Moderate power, digital
Shielded wire harness	50-70 dB	High (multi-axis)	>20A per wire	High power, RF

Mating connectors represent another critical EMI vulnerability point in flex cable systems. Standard FPC connectors often lack sufficient ground pins to maintain consistent reference planes across the interface, creating impedance discontinuities that can radiate emissions or allow external interference to couple into the system.

- **Ground pin interleaving:** Place ground pins around digital pins in the pinout to ensure a reference return path
- **Impedance matching:** Input impedance through the connector should match the input trace impedance
- **Shield termination:** 360° shield termination preferred over pigtail connections
- **Ferrite placement:** Common mode chokes within 1” of connector interface

Custom flex PCB designs become necessary when standard solutions cannot achieve required hatch density or when specific impedance matching is needed for sensitive RF applications.

- **Ferrite cores:** Type 31 material for 1-300 MHz, Type 43 for 25-300 MHz
- **Filter modules:** Multi-stage higher order LC filters
- **Common mode chokes:** Impedance >1 kΩ for common-mode noise
- **Shielding gasket:** High shielding effectiveness for enclosure interfaces

Power distribution through flex interconnects presents additional challenges, as switching supplies can inject common mode noise that radiates from inadequately shielded connector interfaces. Custom cable assemblies allow strategic placement of EMI suppression components that standard flex ribbons cannot accommodate.

DESIGN GUIDELINES AND DECISION FRAMEWORK FOR MISSION-CRITICAL APPLICATIONS

Selecting the optimal interconnect solution for military and aerospace systems requires systematic evaluation of mission requirements against technical capabilities and risk factors. The decision framework must prioritize reliability and performance over cost considerations, as field failures in defense applications carry consequences far beyond component replacement costs.

Application Requirements	Standard Flex Ribbon	Hatched Ground Flex PCB	Wire Harness
High pin density (>100 pins)	Excellent	Excellent	Poor
Multi-axis routing flexibility	Poor	Fair	Excellent
High power (>10A)	Poor	Fair	Excellent
Extreme temperature (-55°C to +125°C)	Fair	Good	Excellent
Field maintenance capability	Poor	Poor	Excellent
EMI shielding (>50 dB)	Poor	Good	Excellent
Space constraints (<5mm height)	Excellent	Good	Poor

Risk Mitigation Strategies:

- **Redundancy planning:** Design dual-path interconnects for critical signal paths
- **Qualification testing:** Perform accelerated life testing beyond standard commercial requirements
- **Supply chain management:** Maintain approved vendor lists with multiple sources
- **Design margin:** Derate current and voltage specifications by 50% minimum
- **Environmental protection:** Specify conformal coatings and sealed connectors for harsh environments

Progress towards higher power density and data rates is driving use of newer flex materials, such as liquid crystal polymer substrates. Interconnects on these materials can operate with higher bandwidth and thus support higher data rates compared to traditional polyimide due to their lower Dk value for the flex materials. However, these components still cannot support the very high data rates found in some high-density connector and cable systems, where supported data rates reach into the 10’s of GHz.

AN OVERVIEW OF COAX LIMITERS FOR USE IN HF SYSTEMS

George Kauffman
PE & CTO, NexTek, LLC

An Overview of Coax Limiters for use in HF Systems Designed to Protect against High Intensity Radiated Fields (HIRF) and other External Electromagnetic Environmental (EME) Elements Using a 20dBm 1-100MHz Limiter

OVERVIEW

Critical communication and instrumentation lines subjected to very high energy RF pulses require RF limiters with exceptionally high pulse power capability. A discussion of a typical high frequency (HF) commercial off the shelf (COTS) limiter manufactured and tested by NexTek is presented to provide insight and understanding of specifications. Data will be presented from an SMA limiter shown in **Figure 1** that has an in-band operating range of 1MHz to 100MHz and is capable of handling pulse RF currents of more than 50 amperes for 10 microsecond pulses.

> *Bulkhead mountable shielded enclosure approximately 2 inches long with stainless steel SMA Female – SMA Female connectors. VSWR ~1.1; Insertion Loss ~0.5dB with power rating of 20dBm and a max peak pulsed power rating of 10kW at 0.5% duty cycle and 26dBm Flat Leakage.*

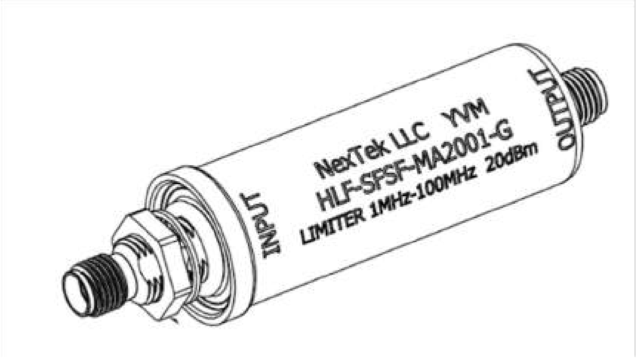


Figure 1: HF Limiter SMA-SMA

RF limiters are used to limit the RF power on a circuit. They are also used to protect sensitive receivers from damage due to excessive input power. Receive circuits, including LNAs, are very susceptible since they are designed for very low-level input signals which are then amplified.

In normal operation, the limiter represents low insertion loss to the in-band signal. However, when there is a higher power level at the input of the LNA (in-band and out-of-band), particularly one that could damage the LNA, the limiter reduces the power level so that the LNA and other components on the receiver are not damaged.

There are several common causes of higher than desired electrical energy on an RF circuit. These include antenna exposure to high RF fields, which is usually due to colocation or proximity to radar under boresight conditions or other high-power transmitters, RF or circuits that normally handle high RF power, such as manufacturing heating, welding, surface treatment, or non-destructive testing, and environments where there is research using plasma physics, accelerators, fusion, and magnetic diagnostics can present out of band energy that can couple into systems.

The electric field exposure varies by application and environment, and the magnitude of those levels are outside the scope of this discussion. Typically, an electric field value in V/m is specified by the environment and then a coupling current factor is derived to get a direct current pulsed injection value. How HIRF exposure direct current injection values are derived are complex in nature and subjective as assumptions and specific systems vary widely. A simple example of estimating the coupled energy into a system due to lightning strikes has been presented previously (Kauffman & Raina, 1996) and can be used as a guide into more complex electric field coupling calculations.

A commonly high electric field value referenced is MIL-STD-464 **Table 2** (Mil-Std-464C) which has an electric field level of 27kV/m fields at 2.7GHz. An exposed antenna could generate over 50kW of power, provided the antenna is rated at or below this frequency. In other cases, a measurement device might be connected to a circuit capable of similar power. A limiter should protect the receiver or other instruments exposed to high energy fields that are in-band or out-of-band (10kHz-18GHz).

A simplified circuit of a limiter is shown in **Figure 2**. The high power enters on the left side and is connected to a primary diverter. This diverter predominately protects the DC block capacitor. This DC block capacitor forms a high pass circuit, defining the lower frequency range of the limiter. There is a second stage limiter after the DC block. There are further impedances in series, followed by a final limiter stage. This final limiter is shown consisting of two diodes. The resulting action of the limiter circuit is reducing the RF voltage and power at the low power output side. In general, the stages are coordinated, so that the voltage levels are reduced for each subsequent stage of the circuit.

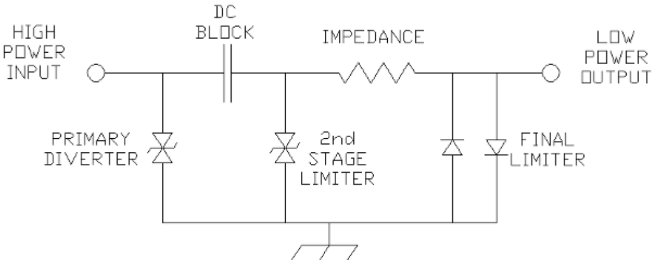


Figure 2: Simplified Schematic

GENERAL CHARACTERISTICS

Steady State Parameters

In normal operation, the limiter should have a good VSWR, low Insertion Loss (IL) and not degrade signals that are under the max operational power rating. However, limiters often have higher insertion loss than typical surge protectors and loses should be included in the systems RF link budget accordingly. **Figure 3** and **Figure 4** show the VSWR and IL for the HF and have similar signatures to that of a band pass filter.

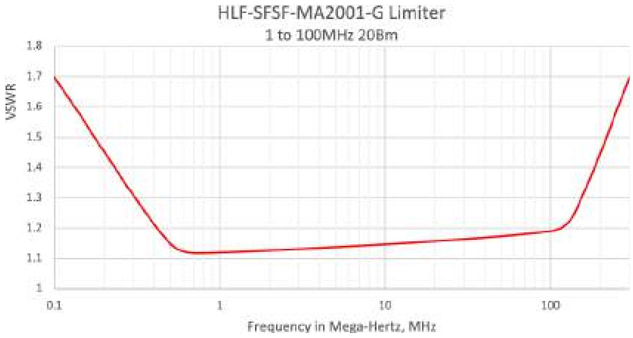


Figure 3: VSWR vs Frequency Plot

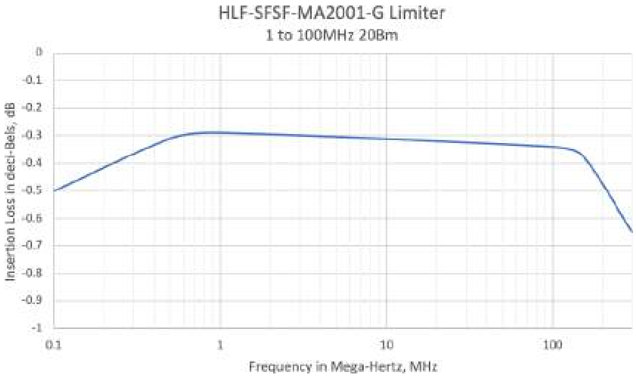


Figure 4: Insertion Loss vs Frequency

DEFINITIONS

Common terms and definitions associated with limiters are presented as an introductory discussion.

Frequency Range: Limiters operation is usually defined by the frequency band. Some RF parameters, including Insertion Loss and VSWR are not defined out of band, however a good limiter will provide limiting functionality significantly out of band to protect against co-located adjacent band transmitters.

RF Rated Power (RF Watts CW): The maximum power rating in this example is 20dBm. This level of power is power can continuously flow through the limiter to the LNA. The RF is single frequency and within the operating band.

Insertion Loss: Within the operating band, the insertion loss is usually less than about 0.5dB, this insertion loss is only seen in the operation band and at RF powers below the RF Rated Power rating.

1dB (-1dB) Compression Power: The input power level where the output power has decreased by 1dB from the normal operating loss. This additional signal loss is called signal compression.

Flat Leakage: Indicates the steady state energy that appears at the output of the limiter and is approximately constant.

Spike Leakage: Indicates the short duration and higher level of energy that appears at the output of the limiter that is substantially elevated above the flat leakage region.

Transition Region: The region above the max operating power that includes the 1dB compression point. The transition region starts with the rated power and continues until the limiter is fully activated by high RF energy.

Pulse Operation Region: When the pulse duration for a current pulse exceeds maximum time, requiring pulsing at a maximum duty cycle. This power level is usually about 6dB to 10dB above the rated power.

Flat response is the somewhat steady state output power level, while spike leakage is a much shorter duration output. Since flat leakage is nearly constant, the units used most often are dBm into a 50 Ohm load. Spike leakage is best referred to as the energy deposited into a 50 Ohm output load and is usually in nano-Joules. Spike leakage can also be reported in peak volts, but this lacks the time element that is captured better in energy.

Pulse Performance

The power transfer function of a typical limiter is shown in **Figure 5**. There are usually three modes of operation. The continuous operation region up to the rated power level, shown in the figure below as 20dBm (~6.33 Vpeak to peak). In this region, the VSWR and Insertion loss parameters are substantially constant. As more power is applied, the limiter begins functioning, and the insertion loss can increase by and additional 1dB. The limiting circuits are just beginning to work at this level of RF voltage. This response is similar to the knee in a Zener diode. The 1dB compression power is usually about 2dB or 3dB above the maximum rated RF power. The limiter might be operated for the long term at this level of power, but it is not advised, since there is no margin for additional power RF power fluctuations or temperature variations.

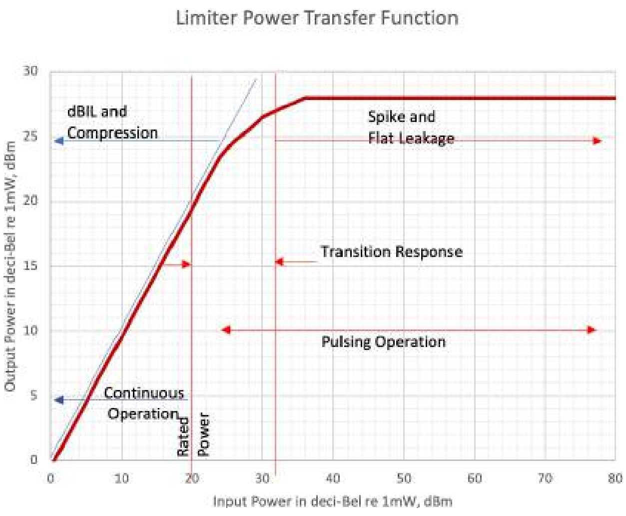


Figure 5: RF Power Transfer Function

When power is dramatically increased, above about 32dBm (~25V pk-pk) the limiter is usually fully functioning. Substantial increase in input power will have minimal effect on the limited output power. There is a region between the rated power and the full limiting operation, where response is transitional, sharing both characteristics.

High Input RF Energy Response Details

The output response of the 20dBm rated limiter with a 700MHz 100W Signal is shown in **Figure 6**. The Flat Response voltage is the average of the plateau of power (and voltage) that is about 3.3 Vpeak or about 0.22W peak. The spike leakage is where the power exceeds the flat leakage by a factor of 2.5, or where the power exceeds 0.55W peak (or the voltage exceeds 10.5Vpk-pk). The spike leakage signature can vary with different frequency units and can be expressed in terms of power or energy.

The energy curve (in red) shows a well-defined flat leakage of 0.22Wpeak (20.8 dBm) after about 1.5 microseconds. A spike leakage is energy above 0.55Wpk, and most energy is confined to the 0.2 to 0.4 microsecond time interval.

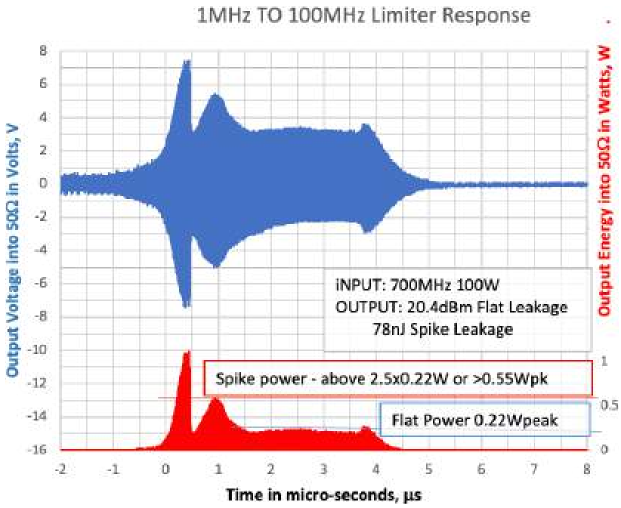
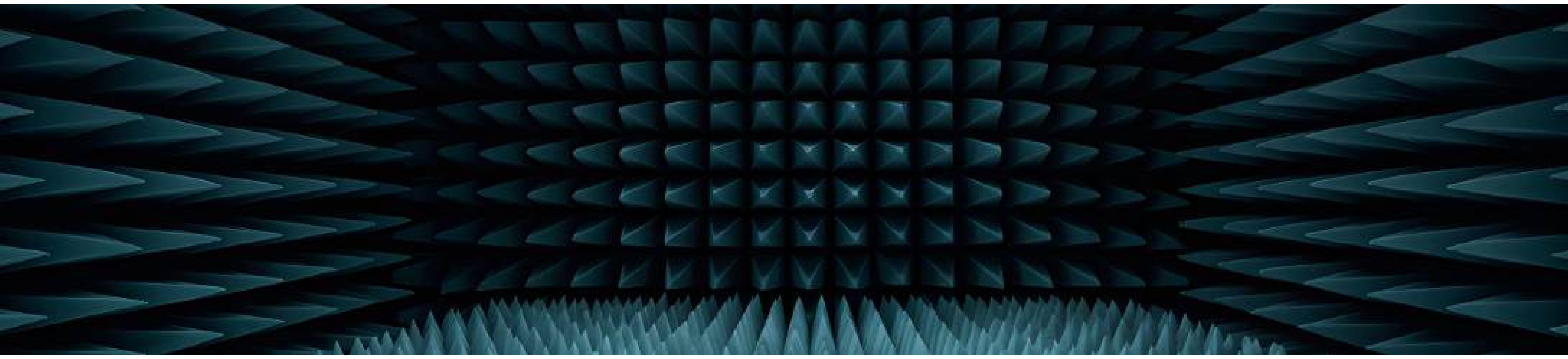


Figure 6: Output Voltage (100W-700MHz Input)

A look at the output voltage signatures and voltage levels of the limiter at different power levels provide further examples of transient response characteristics. **Figure 7** through **Figure 10** show the output response as the power level increases from normal operation and incremental power increases. A 10usec pulse of 700MHz is used for these increasing power pulses example. While **Figure 11** shows the output response of a 10usec 2.2GHz input pulse.



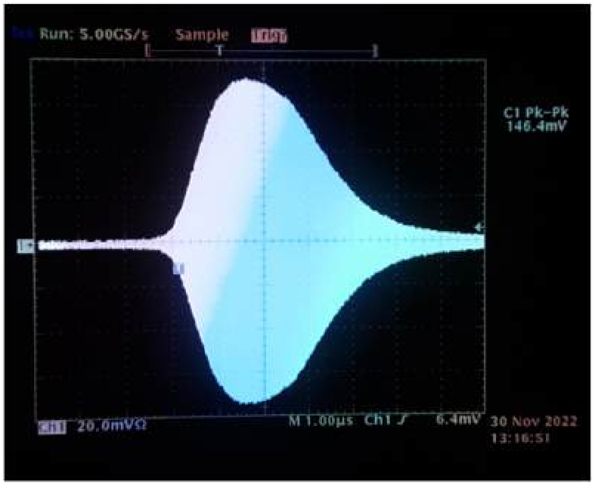


Figure 7: Output - 30dBm Input

The curve shows a 1MHz to 100MHz 20dBm rated limiter, with a 700MHz input pulse of 30dBm, limited to about 27.3 dBm (~14.6Vpk-pk) at the output, or about 2.7dB compression.

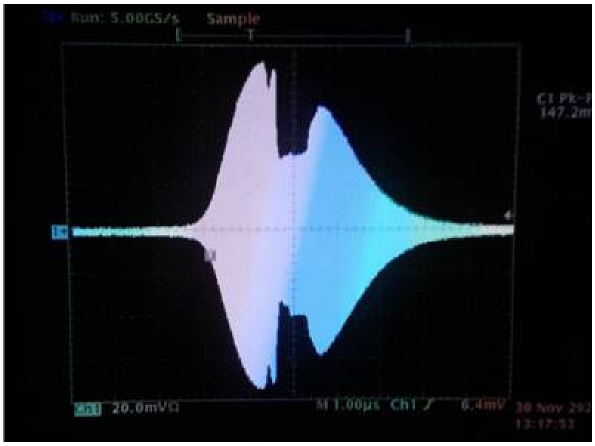


Figure 8: Output 33dBm Input

If the 700MHz power is increased to 33dBm, the flat leakage region just begins to form, as shown by the voltage reduction in the middle of the pulse. The initial response of about 14.6Vpk-pk is followed by a region of about 18.5dBm flat leakage.

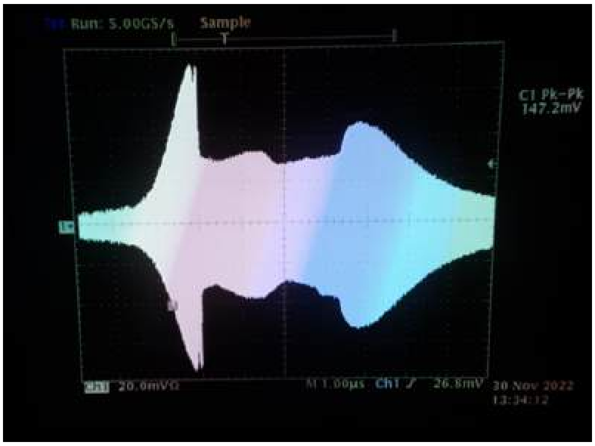


Figure 9: Output 48dBm Input

Increasing the 700MHz pulse power to 48dBm, the output power pulse magnitude stays nearly constant, however the 18.5 dBm flat leakage duration increases.

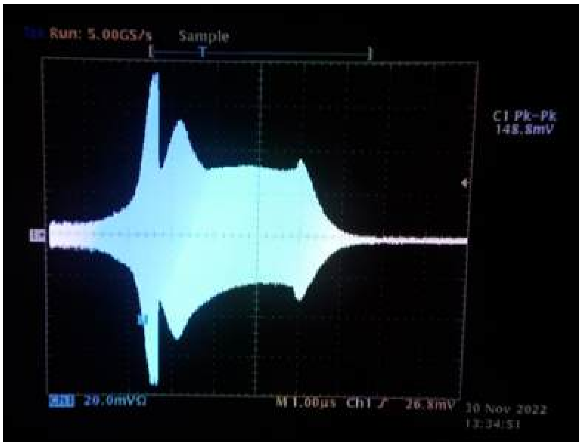


Figure 10: Output 50dBm Input

Increasing the 700MHz pulse power further to 50 dBm, the initial spike and flat leakage magnitudes are similar to lower input pulses, but the pulse duration is shorter.

Pulsing the limiter with 50dBm at 2.2GHz, we see an output of 21.1dBm. The spike leakage and transition phenomena do not occur at this test condition.

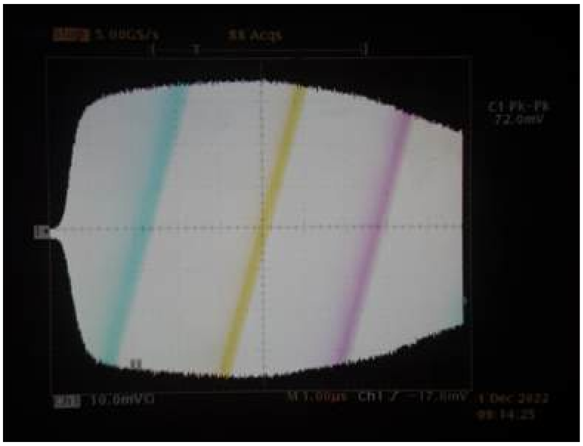


Figure 11: Output 50dBm 2.2GHz Input

Limiters have a maximum pulse width versus input power level that is primarily a function of power dissipation and resulting temperature rise. This usually assumes a 25ºC initial temperature. This HF limiter has a maximum power equivalent level over 100kW for pulses less than 10 microseconds. **Figure 12** presents the single pulse power versus maximum pulse width for this device for pulse power above the blue curve, duty cycle effects, or off time, must be used to reduce the average power. This represents the pulse limitation where off time needs to be used to prevent excessive temperature rise of the limiter. The concept of pulse current is introduced here. To best capture the quality and effectiveness is to rate the limiter to input current. While the RF power might usually be measured at 50 Ohms, the limiter is not close to 50 Ohms when in the limiting mode. In addition, RF amplifiers or other sources can usually have much lower impedance than 50 Ohms. Therefore, the current can vary, depending upon the source or generator, and the limiter. To provide predictable performance, the capacity of the limiter is best related to the input pulse current levels. This figure can also be used to convert RF Watts to Current. The cumulative effects of a series of several pulse currents needs to be considered and modeled.

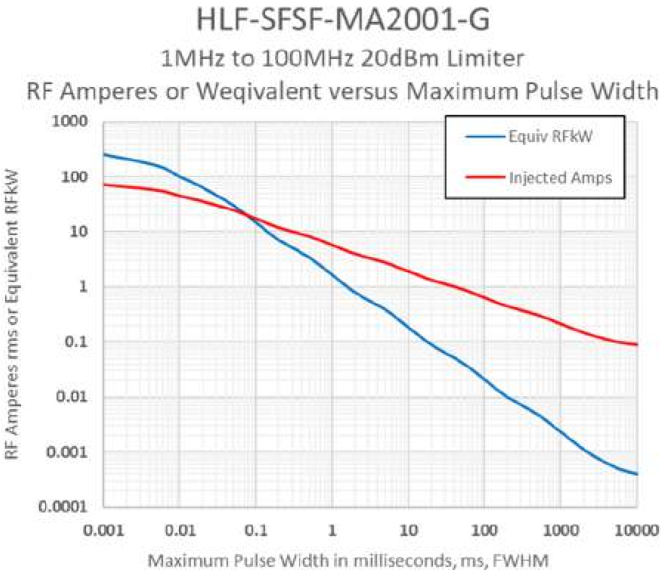


Figure 12: Power versus Pulse Width

The limiter duty cycle versus injected pulse current is shown in **Figure 13**. This graph is another way to view the need to modulate or allow quiescent time for the limiter. Pulse currents must be limited by the duty cycle (the pulse duration divided by the usually longer off time). The cumulative effects of pulse trains of varying currents and pulse widths needs to be considered and modeled.

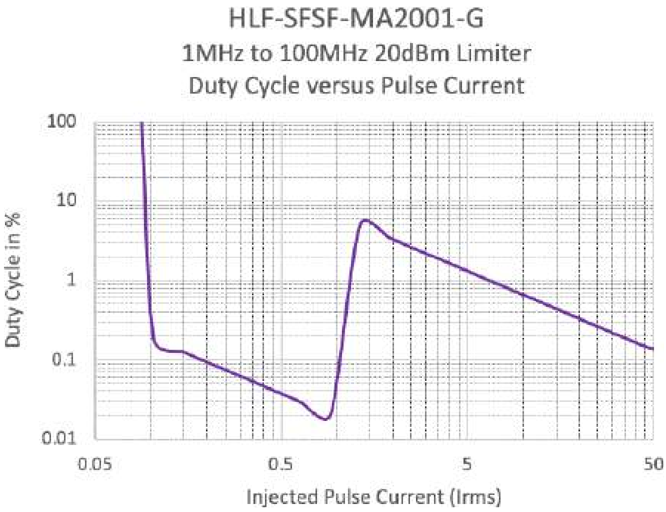


Figure 13: Duty Cycle versus Pulse Current

SUMMARY

The information presented along with measured lab results provide an introductory explanation of the performance of Nextek's high-performance HLF series limiters designed for high energy environments. A systems engineer needs to consider many variables to fully determine the threat level and protection level requirements to ensure the limiter is providing the protection desired. Direct current injection testing is a good indicator of how a device will perform. Testing across duty cycle, pulse widths, frequency and power levels can be expensive and time consuming. The results presented in this paper provide a glimpse into what one would expect to see as they do their own testing.

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CUBESATS REQUIRE SPECIAL ESD HANDLING PROTOCOLS FOR LAUNCH INTEGRITY — PART I

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CubeSats are relatively inexpensive when compared to traditional vehicle-size satellites. Since their inception, CubeSat spacecraft have shown functional success rates ranging from 40% to 75% for launch and deployment phases.

Figure 1: Tu-Pod in Space[1]

According to the International Journal of Aerospace Engineering, CubeSat deployment success rates now exceed 75%. In 2017, mission failures stood at 50%. Closing the gap from 25% to 0% may be achieved by implementation of electrostatic discharge (ESD) control measures. One must ask whether NASA-STD-8739.6B, Section 7, protocols for ESD compliance in low relative humidity (RH) and extreme conditions are sufficiently in place to ensure best value for the taxpayer.

Since 2022, the manufacture of vertical transport field effect transistors (VTFETs) has exponentially increased transistor count for devices, now commercially available. Apple's M1 Ultra contains 114 billion transistors compared to Intel's 4004 microprocessor introduced in 1971 (see **Table 1**) at 2,300 transistors.[2]

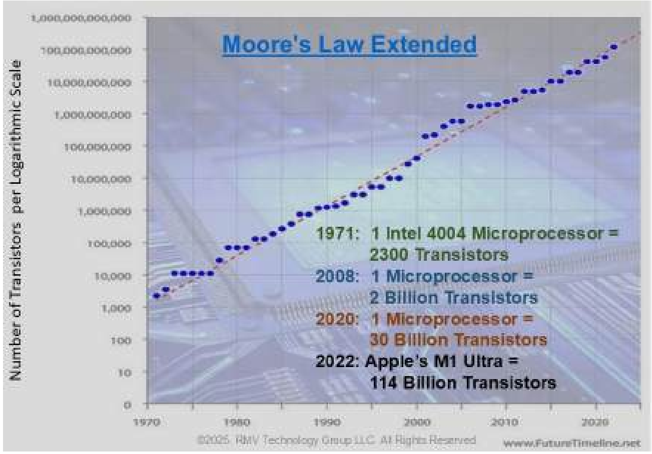

Table 1: Historical Transistor Count Comparison

GOES-R Satellite weighs 6,299 lbs., compared to a CubeSat 1.0 at 3 lbs., as shown in **Figures 2** and **3**.

Figure 2: GOES-R Satellite

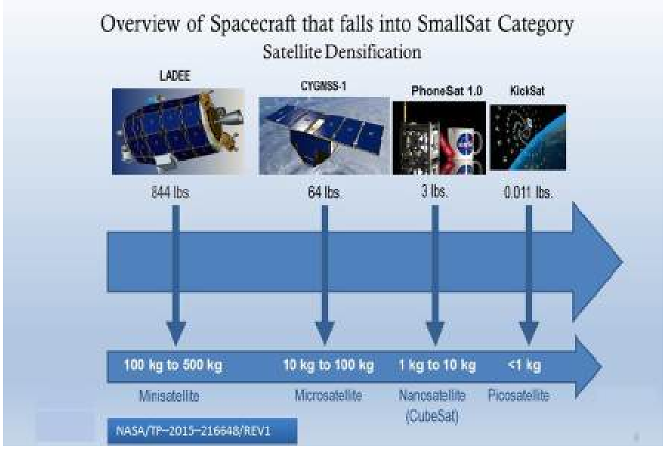

Figure 3: CubeSat 1.0

Due to microprocessor densification via VTFET-manufactured ESD-sensitive devices (ESDS), a swarm of 5 to 8 CubeSats in less than 10 years could replace a 2 to-3-ton satellite. Traditional ESD protective mechanisms for ESDS will require strengthening of ESD procedures in the EPA to safely handle Class 0Z (<±50 volts) components.

Without a doubt, "speed kills" with microprocessor densification. One can no longer rely upon internal ESDS protection mechanisms without implementing an ESD control program. Moreover, the author has reviewed CubeSat design specifications that incorporate ESD-sensitive devices, and often these requirements have overlooked ESD procedures to safeguard Class 0Z devices.

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[1] Courtesy Amin Djamshidpour, Co-Founder Teton Aerospace.

[2] NASA STD 8739.6; 6.1 TEMPERATURE AND RELATIVE HUMIDITY (RH).

JPL has taken cleanliness and ESD control for their interplanetary CubeSats to a different level by redesigning a dedicated 1,250 square foot room — comparable to a modern high bay inspired by Moore's Law — from an existing program. Many governmental, university, and commercial SmallSat manufacturers appear to have overlooked ESD procedures during CubeSat construction by using desktop or non-flight hardware surfaces without implementing static control safeguards.

CubeSat builds placed on charge-generating Plexiglas or Lexan platforms can facilitate field-induced model (FIM) discharges. Incorporation of an ANSI/ESD STM4.1 approved work surface (**Figure 4**) is required to protect today's flight hardware Class 0Z devices at <±50 volts (see **Table 2**).

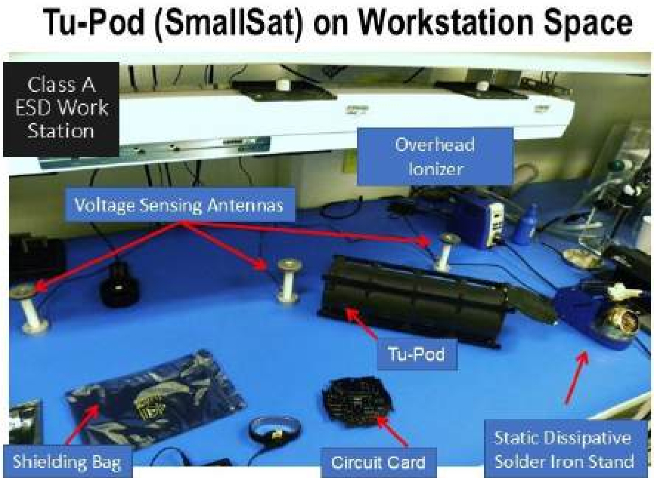

Figure 4: ANSI/ESD STM4.1-compliant ESD work surface

ANSI-ESDA-JEDEC JS-001

HBM Classification	Voltage (± V)
0Z	<50 [Space & Defense]
0A	50 - <125
0B	125 - <250
1A	250 - <500
1B	500 - <1000
1C	1000 - <2000
2	2000 - <4000
2A	4000 - <8000
2B	≥8000

Table 2: ESD Susceptibility Classes and Thresholds

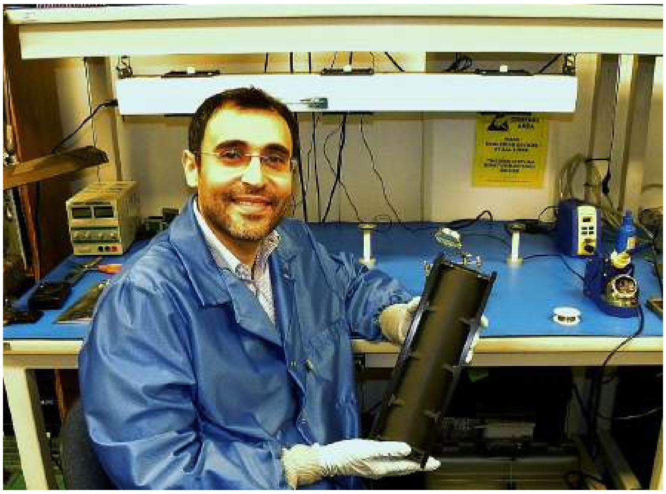

Figure 5: Amin Djamshidpour, Teton Aerospace

Adherence to static control protocols in compliance with NASA-STD-8739.6B, Section 7, is mandatory when building CubeSats. NASA-STD-8739.6B, Section 7, and MIL-STD-2073, apply during test, inspection, transport, and handling of electronic parts, assemblies, and equipment susceptible to ESD damage greater than or equal to 100 volts HBM, 200 volts CDM, and 35 volts on isolated conductors. NASA-STD-8739.6B, Section 7, along with the prime contracting community, takes precedence over other Industry Standards for ESD integrity in low RH and extreme environmental conditions.

An unfounded belief is that some commercial off-the-shelf (COTS) components are not Class 0Z. Classification for ESD-sensitive EEE parts has been equally applied to COTS and government off-the-shelf (GOTS). COTS are ready-made and cheaper to use, whereas GOTS are intended for internal use by the US Government. To comply with NASA-STD-8739.6B, Section 7, one must have technical justification to downgrade practices or obtain a waiver.

Product qualification of ESD materials must conform to NASA-STD-8739.6B, Section 7, using traceable technical data, in-house or third-party testing with instrumentation specified by ANSI/ESD Standards or Standard Test Methods. For in-house qualification, the on-site qualifier must conduct testing of ESD materials at 0% RH in support of NASA's ongoing academia-funded CubeSat programs for low earth orbit (LEO) and deep space exploration.

For aerospace and defense, it is not uncommon to build and assemble products in Class A (<±35 V) ESD protected areas. This is illustrated in **Figures 4** and **6**.

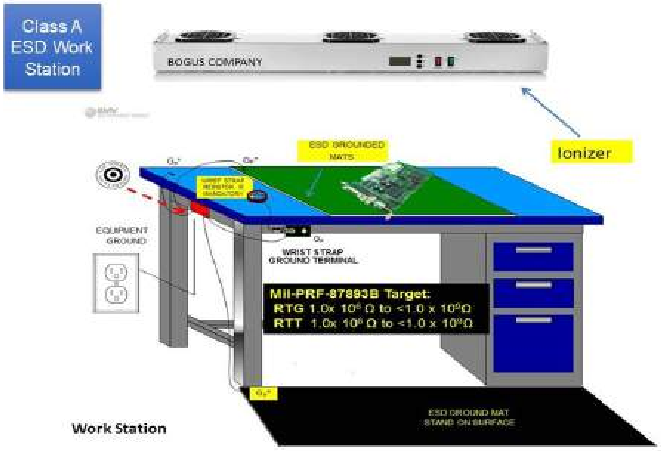

Figure 6: RMV Laboratory at NASA Ames Research Park

An ANSI/ESD STM4.1 workstation is certified annually with periodic verification as outlined in the agency's ESD Procedures.

Certification labels are affixed to the work surface, ionizers, flooring mat, static control chair, soldering iron, wrist strap monitor, and proximity voltage sensing antennas. Quantitative data must be recorded rather than using simple pass/fail statements.

Figure 7: Operator setup for ESD-sensitive handling

As illustrated (**Figure 7**), the operator, engineer, or scientist gowns up and tests the ANSI/ESD S1.1 grounded wrist strap. The wrist strap is connected to ground; the cleanroom ANSI/ESD STM15.1 approved nitrile gloves are donned after turning on the ionizer. In this case, an ESD Type 1 moisture barrier bag is then opened, housing a Tu-POD circuit card. Upon completion, the static ESD-sensitive device (circuit card) is placed into a Type I bag (**Figure 9**).

Figure 8: Opened Type I barrier bag

Figure 9: Re-sealed circuit card in Type I bag

When CubeSat manufacturers handle Class 0Z items (<±50 volts HBM), additional mitigation techniques should be adopted:

1. Maintain RH between than 40% and 60%, and monitor RH in the EPA
2. Use groundable ESD garments (overalls) with elastic wrist cuffs
3. Use steady-state DC ionization with offset voltage <±35 V
4. Use both dual-cord audio jack wrist strap and ESD-safe shoe or sole grounding straps
5. Operators seated in ESD chairs must wear wrist straps
6. Qualify all ESD protective packaging before use on ESD work surfaces
7. Remove all non-process insulators from the work area

Special Recognition to Amin Djamshidpour, Co-Founder Teton Aerospace, amin@tetonsys.com

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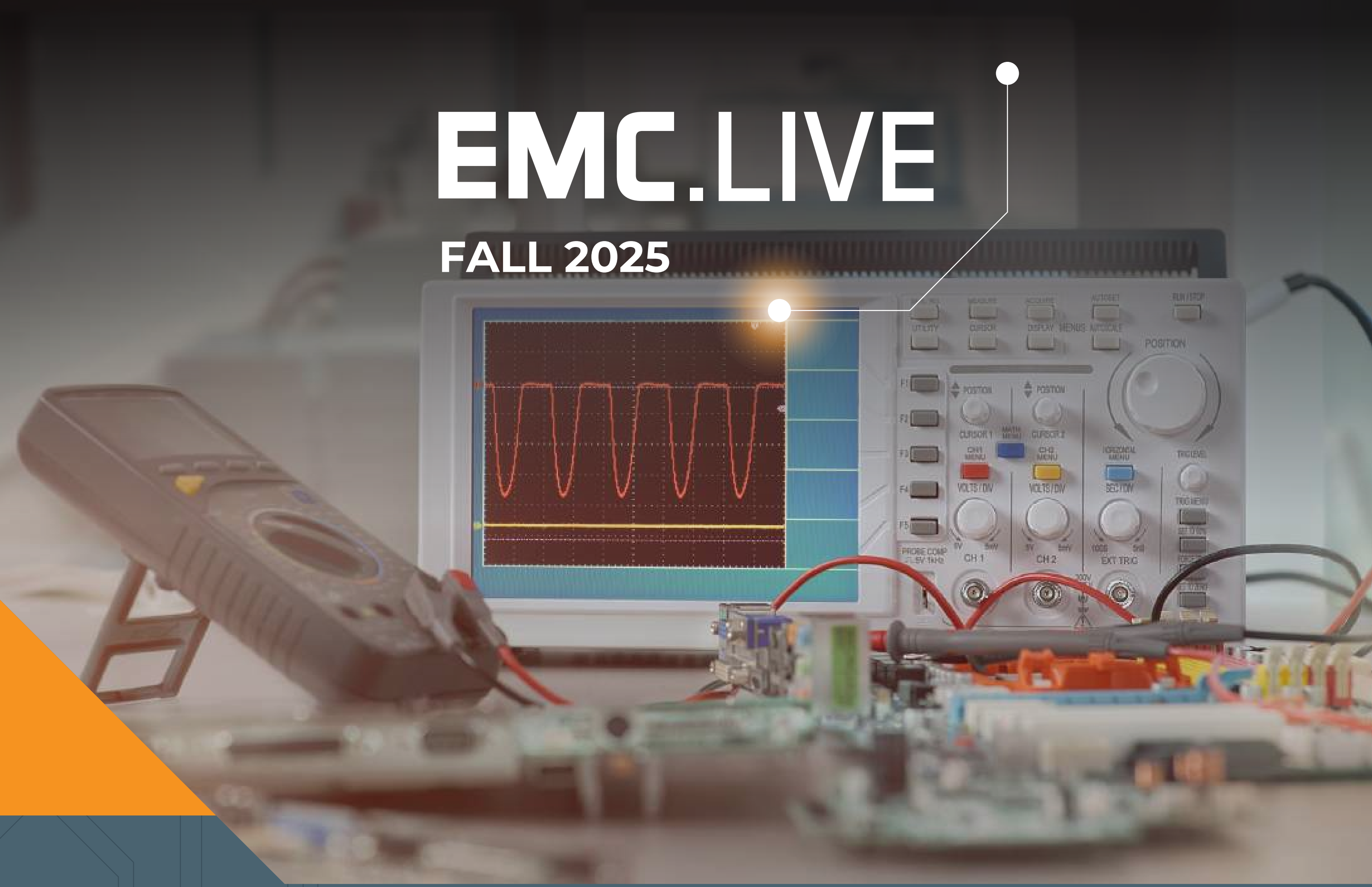

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