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He is the author of the third edition of the 1,157-page book Electromagnetic Compatibility, Methods, Analysis, Circuits, and Measurement published by CRC press in 2017, as well as numerous papers of a practical nature.

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2024 EMC SUPPLIER GUIDE

Introduction

In this section, we provide a quick guide to some of the top suppliers in each EMC category–test equipment, components, materials, services, and more. To find a product that meets your needs for applications, frequencies, standards requirements, etc., please search these individual supplier websites for the latest information and availability. If you have trouble finding a particular product or solution, email info[@](mailto:info%40interferencetechnology.com?subject=)interferencetechnology.com for further supplier contacts.

DESIGN FOR COMPLIANCE ESSENTIALS

Kenneth Wyatt

Wyatt Technical Services

INTRODUCTION

While unrealistic to discuss all aspects of product design in a single article, I'll try to describe the most common design issues I find in the hundreds of client products I've had a chance to work on. These issues generally include PC board design, cables, shielding, and filtering. More detailed information may be found in the reference section at the end of this article.

The top three product failures I run into include (1) radiated emissions, (2) radiated susceptibility, and (3) electrostatic discharge. Other failures can include things like conducted emissions, electrically fast transient, conducted susceptibility, and electrical surge. Most of these last items are also the result of the same poor product designs, which cause the top three failures.

NOTE: I prefer to avoid the word "ground" in this article or in my consulting practice. The reason is that there are too many misinterpretations, which can also lead to EMC failures. It's much clearer to use power and power return, and signal and signal return – or just "return plane" or reference plane. Finally, cable shields or shielded enclosures are "bonded" together – not "grounded". The only exception is the so called "safety ground" or earth ground. But these have nothing at all to do with proper EMC design – just personal safety against electrical shock. I suppose the one exception would be the earth ground connection on a three-wire power line filter. Also, occasionally, there will be an earth ground on a PC board, especially for power supplies. However, connecting a product or system to earth ground *will not improve EMI due to the very high inductance (length) of the wire.*

PC BOARD DESIGN

The single most important factor in achieving EMC/EMI compliance involves the printed circuit board design. It's important to note that not all information sources (books, magazine articles, or manufacturer's application notes) are correct when it comes to designing PC boards for EMC compliance – especially sources older than ten years, or so. In addition, many "rules of thumb" are based on specific designs, which may not apply to future or leveraged designs. Some rules of thumb were just plain lucky to have worked.

PC boards must be designed from a physics point of view and the most important consideration is that high frequency signals, clocks, and power distribution networks (PDNs) must be designed as transmission lines. This means that the signal or energy transferred is propagated as an electromagnetic wave. PDNs are a special case, as they must carry both DC current and be able to supply energy for switching transients with minimal simultaneous switching noise (SSN). The characteristic impedance of PDNs is designed with very low impedance (0.1 to 1.0 Ohms, typically). Signal traces, on the other hand, are usually designed with a characteristic impedance of 50 to 100 Ohms.

The previous article introduced the concept of the circuit theory and field theory viewpoints. A successful PC board design accounts for both viewpoints. Circuit theory suggests that current flows in loops from source to load and back to the source. In many cases of product failure, the return path has not been well defined and, in some

cases, the path is broken. Breaks or gaps in the return path are major causes of radiated emissions, radiated susceptibility, and ESD failures.

Correspondingly, electric fields on PC boards exist between two pieces of metal, such as a microstrip, over a return plane (or trace). If the return path is broken, the electric field will "latch on" to the next closest metal and will not likely be the return path you want. When the return path is undefined, then the electromagnetic field will "leak" throughout the dielectric space and cause common mode currents to flow all over the board, as well as cause cross-coupling of clocks or other high speed signals to dozens of other circuit traces and vias within that same dielectric.

Figure 1 shows a propagating wave within the dielectric space between the signal trace and return plane (or trace). This shows both the conduction current flowing in the signal trace and back on the return plane (or trace) and the displacement current "through" the dielectric.

The signal wave front travels at some fraction of the speed of light as determined by the dielectric constant. In air, signals travel at about 12 inches per nanosecond. In the typical FR4 dielectric, the speed is about half that at 6 inches per nanosecond. Refer to Reference 1, 2, and 3 for more information on the physics of signal propagation through PC boards.

In order to satisfy both the circuit and field theory viewpoints, we now see the importance of adjacent power

Electromagnetic Wave (Digital Signal) Propagation in PC Boards

Conduction current travels along the inside surface of the microstrip and ground reference plane.

Displacement current appears to "flow" through the dielectric space between the copper.

Figure 1: Cross section of a propagating wave guided by a microstrip and reference plane.

and power return planes, as well as adjacent signal and signal return planes. PDN design also requires both bulk and decoupling "energy storage" capacitors.

The bulk capacitors 4.7 to 10 μF, typ.) are usually placed near the power input connector and the decoupling capacitors (1 to 10 nF, typ) nearest the noisiest switching devices – and, most importantly, with minimal trace length connecting these from the power pins to signal return plane. Ideally, all decoupling capacitors should be mounted right over (or close to) the connecting vias and multiple vias should be used for each capacitor to reduce series inductance.

Signal or power routed referenced to a single plane will always have a defined return path back to the source. *Figure 2* shows how the electromagnetic field stays within the dielectric on both sides of the return plane. The dielectric is not shown for clarity.

Figure 2: A signal trace passing through a single reference plane.

On the other hand, referring to *Figure 3*, if a signal passes through two reference planes, things get a lot trickier. If the two planes are the same potential (e.g., both are return planes), then simple connecting vias may be added adjacent to the signal via. These will form a nice, defined return path back to the source.

If the two planes are differing potentials (for example, power and return), then stitching capacitors must be placed adjacent to the signal via. Lack of a defined return path will cause the electromagnetic wave to propagate throughout the dielectric, causing cross coupling to other signal vias and leakage and radiation out the board edges as shown.

Figure 3: A signal trace passing through two reference planes. If the reference planes are the same potential (signal or power returns, for example), then stitching vias next to the signal via should be sufficient. However, if the planes are different potentials (power and return, for example), then stitching capacitors must be installed very close to the signal via. Lack of a defined return path will cause the electromagnetic field to leak through the dielectric, as shown, and couple into other signal vias or radiate out board edges.

For example, let's take a look at a poor (but very typical) board stack-up that I often see. See *Figure 4*.

Notice the power and power return planes are three layers apart. Any PDN transients will tend to cross couple to the two signal layers in between. Similarly, few of the signal layers have an adjacent return plane. Therefore, the propagating wave return path will jump all over to whatever is the closest metal on the way back to the source. Again, this will tend to couple clock noise throughout the board.

Figure 4: A six-layer board stack-up with very poor EMI performance.

Figure 5: A six-layer board stack-up with good EMI performance. Each signal layer has an adjacent return plane and the power and power return planes are adjacent.

A better design is shown in *Figure 5*. Here, we lose two signal layers, but we see the power and power return planes are adjacent, while each signal layer and routed power has an adjacent signal (or power) return plane. It's also a good idea to run multiple connecting vias between the two return planes in order to guarantee the lowest impedance path back to the source. The EMI performance will be significantly improved using this or similar designs. In many cases, simply rearranging the stack-up is enough to pass emissions.

Note that when running signals between the top and bottom layers, you'll need to include "stitching" vias between the return planes and stitching capacitors between the power and power return planes right at the point of signal penetration in order to minimize the return path. Ideally, these stitching vias should be located within 1 to 2 mm of each signal via.

Other Tips - Other design tips include placement of all power and I/O connectors along one edge of the board. This tends to reduce the high frequency voltage drop between connectors, thus minimizing cable radiation. Also, segregation of digital, analog, and RF circuits is a good idea, because this minimizes cross coupling between noisy and sensitive circuitry.

Of course, high-speed clocks, or similar high-speed signals, should be run in as short and as direct a path as possible. These fast signals should not be run long board edges or pass near connectors.

Gaps in Return Plane - I'd like to come back to the gap or slot in the return plane mentioned earlier and show an example of why it's bad news for EMI. When the return path is interrupted, the conduction current is forced around the slot, or otherwise finds the nearest (lowest impedance) path back to the source. The electromagnetic field is forced out and the field will "leak" throughout the board. I have an article and good demonstration video of this and how it affects common mode currents and, ultimately, EMI. See *Figure 6* and Reference 4.

Figure 6: A demonstration test board with transmission lines terminated in 50 Ohms. One transmission line has a gap in the return plane and the other doesn't. A 2 ns pulse generator is connected to one of the two BNC connectors in turn and the harmonic currents in a wire clipped to the return plane are measured with a current probe

The difference between the gapped and un-gapped traces is shown in *Figure 7*. Note the harmonic currents are 10 to 15 dB higher for the gapped trace (in red). Failing to pay attention to the signal and power return paths is a major cause of radiated emissions failures.

SHIELDING

The two issues with shielded enclosures are getting all pieces well-bonded to each other and to allow power or I/O cable to penetrate it without causing leakage of common mode currents. Bonding between sheet metal may require EMI gaskets or other bonding techniques. Slots or apertures in shielded enclosures become issues when the longest dimension approaches a half wavelength.

Figure 7: The resulting common mode currents on an attached wire as measured with a current probe. The trace in aqua is the un-gapped return path and the trace in red, the gapped return path. The difference is 10 to 15 dB higher for the gapped return path. These harmonic currents will tend to radiate and will likely cause radiated emissions failures.

Figure 8 shows a handy chart for determining the 20-dB attenuation of a given slot length. For example, if a product design requires at least a 20-dB shielding effectiveness, then the longest slot length at 1000 MHz can be just one-half inch. See References 5 and 6 for more detail on shielding. *Interference Technology* also has a free downloadable 2016 EMI Shielding Guide with excellent information (Reference 7).

Figure 8: A chart of attenuation versus slot length. Figure courtesy of Henry Ott

Figure 9 is a chart of wavelength versus frequency. For example, a 6-inch (15 cm) slot has a half-wave resonance at 1000 MHz.

Figure 9: A handy chart for determining resonant frequency versus cable or slot length in free space. Half-wavelength slots simulate dipole antennas and are particularly troublesome. Figure courtesy of Patrick André.

Cable Penetration - The number one issue I find when tracking down a radiated emissions problem is cable radiation. The reason cables radiate is that they penetrate a shielded enclosure without some sort of treatment – either bonding the cable shield to the metal enclosure

Figure 10: Penetrating the shield with a cable defeats the shield. This example shows how external energy sources can induce noise currents in I/O cables, which can potentially disrupt internal circuitry. The reverse is also true, where internal noise currents can flow out the cable and cause emissions failures. Figure courtesy of Henry Ott.

Figure 11: Result of a penetrating cable through a shielded enclosure, because of un-bonded I/O connectors to the shielded enclosure.

or common mode filtering at the I/O or power connector (*Figure 10* and *11*). This occurs frequently, because most connectors are attached directly to the circuit board and are then poked through holes in the shield. Once the cable is plugged in, it is "penetrating the shield" and EMI is the usual result.

There are four combinations or cases that must be considered: shielded or unshielded products, and shielded or unshielded cables. Power cables are usually unshielded for consumer/commercial products and so require power line filtering at the point of penetration or at the connector of the circuit board. Shielded cables must have the shield bonded (ideally in a 360-degree connection) to the product's shielded enclosure. If the product does not have a shielded enclosure, then filtering must be added at the

point of penetration or at the I/O connector of the PC board. *Figure 11* shows the usual result when connectors simply poke through a shielded enclosure.

Cable Shield Terminations - Another potential issue is if the I/O cable uses a "pigtail" connection to the connector shell. Ideally, cable shields should be terminated in a 360-degree bond for lowest impedance. Pigtails degrade the cable shield effectiveness by introducing a relatively high impedance. For example, a 1-inch pigtail connection has 12 Ohms impedance at 100 MHz and gets worse the higher you go in frequency. This is especially problematic for HDMI cables, because the HDMI working group (http://www.hdmi.org) originally failed to specify the method for terminating the cable shield to the connector.

FILTERING

I won't go into very much detail here, because *Interference Technology* has an excellent EMI Filter Guide free for the downloading (see Reference 8). Suffice to say, filters, as well as transient protection, are important at power and I/O connectors. Typically, these will be common mode topologies, as shown in *Figure 12.* Most signal-level common mode chokes may be obtained in surface mount packaging. Power chokes are much larger to handle the current and may be obtained as either surface mount or through-hole mount, depending on the current rating. Many Ethernet connectors have built-in common mode filtering.

Power supply input filters are generally designed to suppress both differential and common mode currents. A typical topology is shown in *Figure 13*. The "X" capacitor in combination with the differential inductance is designed to filter differential mode, while the CM choke and "Y" capacitors are designed to filter common mode. The resistor shown is usually 100 kΩ and the purpose is merely to quickly bleed off the line voltage stored on the capacitors to a safe level when unplugged from the line outlet

For general purpose filtering of signals, the handy chart of possible filter topologies may be found in Reference 9 and is reproduced here in *Figure 14*. The appropriate topology

Figure 12: A typical common mode filter used for I/O filtering. The two windings are wound in opposite directions and so tend to cancel the common mode currents. Figure courtesy of Clayton Paul.

Figure 13: A general purpose filter typically used for power supply input filtering.

depends on the source and load impedances. If these impedances are not known, then either the "PI" or "T" topology may be used (#3 or #5 on the chart, respectively).

Ferrite or inductive components should not be used in series with the power pins of ICs, as this will only reduce the ability of the local decoupling capacitors to supply required energy during simultaneous switching of the IC output stages with the resulting higher power supply noise.

Figure 14: Five common filter topologies, depending on the source and load impedances. Figure courtesy of Würth Electronik.

Figure 15: Impedance versus frequency for various types of ferrite materials. Figure, courtesy Fair-Rite Corp.

Ferrite Chokes - One common filter element usually added to I/O cables is the ferrite choke. Ferrite chokes come in either the clamp-on types or solid cores meant to be assembled along with the cable assembly. Often, these are used as a last resort to reduce cable emissions or susceptibility. Most ferrite chokes have an

associated impedance versus frequency characteristic, often peaking around 100 to 300 MHz. Some materials are designed to peak below 100 MHz for lower frequency applications. Maximum impedances can range from 25 to 1000 Ohms, depending on the ferrite material used and style of choke. An example of various ferrite materials and associated impedance curves are shown in *Figure 15*.

Sometimes, clipping a ferrite choke onto a cable has no effect. This is usually due to the fact the choke has the same, or lower, effective impedance than the cable itself. The attenuation of a ferrite choke is easily calculated.

Attenuation (dB) = 20 $*$ log((Zin + Zferrite + Zload) / (Zin + Zload))

For example, if we add a 100 Ohm ferrite choke to a power supply cable with system impedance of 10 Ohms, the attenuation would be:

Attenuation = 20 $*$ log((10 + 100 + 10) / (10 + 10)) = 15.5 dB

Refer to Reference 9 for much additional detail on ferrite chokes and general filter design.

TRANSIENT PROTECTION

In order to protect internal circuitry from electrical transients, such as ESD, electrically fast transient (EFT), or power line surge, due to lightning, transient protective devices should be installed at all power and I/O ports. These devices sense the transient and "clamp" the transient pulse to a specified clamp voltage.

Transient protectors in signal lines must generally have a very low parallel capacitance (0.2 to 2 pF, typical) to the return plane, depending on the data rate in order to maintain signal integrity. These silicon-based devices may be purchased in very small surface mount packaging.

Power line surge protection usually requires much larger transient protection devices and they can come in a variety of types. Gas discharge or metal oxide varistors are the most common, but larger silicon-based devices are also available. More information on the design of surge protection may be found in Reference 6.

SUMMARY

Most EMC/EMI failures are due to poor shielding, penetration of cables through shields, poor cable shield termination, poor filtering, and above all, poor PC board layout and stack-up. Paying attention to these common design faults will pay off with a lower risk of compliance failures and result in lower project costs and schedule slippage.

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BASIC EMC CONCEPTS

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Understanding EMC is all about two important concepts: (1) digital signals are propagated in circuit traces as electromagnetic waves traveling in the dielectric space between the circuit trace and adjacent return plane and (2) the induced currents flow in a loop back to the source.

HOW DIGITAL SIGNALS MOVE

At frequencies greater than about 100 kHz, digital signals start to propagate as electromagnetic waves in transmission lines formed by the circuit trace or stripline and the nearest solid return plane. As shown in *Figure 1*, a high frequency signal propagates along a transmission

line (circuit trace over return plane, for example), and the wave front induces a conduction current in the copper trace and back along the return plane. Of course, this conduction current cannot flow through the PC board dielectric, but the charge at the wave front repels a like charge on the return plane, which "appears" as if current is flowing. This is the same principle for capacitors and Maxwell called this effect "displacement current".

The signal's wave front travels at some fraction of the speed of light, as determined by the dielectric constant of the material (about half light speed, or 6 inches/ns in FR4), while the conduction current is comprised of a high

Electromagnetic Wave (Digital Signal) Propagation in PC Boards

Conduction current travels along the inside surface of the microstrip and ground reference plane.

Displacement current appears to "flow" through the dielectric space between the copper.

density of free electrons moving at the "drift" velocity (<<1 mm/second). The actual physical mechanism of near light speed propagation is due to a "kink" in the E-field, which propagates within the dielectric and guided by the molecules of copper. Refer to References 1 through 4 for further details.

The important thing is that this combination of conduction and displacement current must have an uninterrupted path back to the source. If it is interrupted in any way, the propagating electromagnetic wave will "leak" all around inside the PC board layers and cause "common mode" currents to form, which then couple to other signals (cross-coupling) or to "antenna-like structures", such as I/O cables or slots/apertures in shielded enclosures and cause radiated emissions.

Most of us were taught the "circuit theory" point of view and it is important when we visualize how return currents want to flow back to the source. However, we also need to consider the fact that the energy of the signal is not only the current flow, but an electromagnetic wave front moving through the dielectric, or a "field theory" point of view. Keeping these two concepts in mind just reinforces the importance of designing transmission lines (signal trace with return path directly adjacent), rather than just simple circuit trace routing. The circuit trace can also be defined as a "waveguide".

It is very important to note that all power distribution networks (PDNs) and high frequency signal traces are really transmission lines and the energy is transferred as electromagnetic waves. We'll show what happens when the return path or return plane is interrupted by a gap or slot in the next article. More on PDN design may be found in References 5, 6, and 7.

CURRENTS FLOW IN LOOPS

The problem we circuit designers miss is defining the return path back to the source. We're very careful to show all the interconnects on the schematic and as traces on the PC board layout, but If you think about it, we don't draw the return paths on the schematic diagram – we just show this as a series of various "ground" symbols.

Where we really get in trouble is if there are more than one ground symbol on the schematic. In the case where we need isolated ground returns, great care must be taken to ensure the signal return paths are uninterrupted and that large signals don't use the same return plane (dielectric space) as low-level signals.

So, what is "high frequency"? Basically, anything higher than 100 kHz. For frequencies less than this, the return current will spread out and tend to follow the shortest path back to the source (path of least resistance). For frequencies above this, the return current tends to follow directly under the signal trace and back to the source (path of least impedance).

Where some board designs go wrong is when high dV/ dt return signals, such as large voltage swings from DC-DC switch mode converters, or high current di/dt return signals get comingled with I/O circuit return currents or sensitive analog return currents. We'll dive deeper into PC board design in the next article. Just be aware of the importance of designing defined signal and power conversion return paths. That's why the use of solid return

Figure 2: An example of differential and common mode currents.

planes under high frequency signals and then segregating (or partitioning) digital, power, and analog circuitry on your board is so important.

DIFFERENTIAL MODE VERSUS COMMON MODE CURRENTS

Referring to *Figure 2*, the differential mode current (in blue) is the digital signal itself (in this case, shown in a ribbon cable). As described above, the conduction current and associated return current flow simultaneously as the signal wave front moves along the transmission line formed by the microstrip and return plane.

The common mode current (in red) is a little more complex in that it may be generated in a number of ways. In the figure, the impedance of the return plane results in small voltage drops due to multiple simultaneous switching noise (SSN) by the ICs (ground bounce). These voltage drops induce common noise currents to flow all over the return (or reference) plane and hence, couple into the various signal traces.

Besides SSN, common mode currents can also be created by gaps in return planes, poorly terminated cable shields, or unbalanced transmission line geometry. The problem is that these harmonic currents tend to escape out along the outside of shielded I/O or power cables connected to the board and radiate. These currents can be very small and It takes just 3 to 5 μA of current to fail the FCC class B radiated emission test limit.

SUMMARY

To summarize product design for EMI compliance, a properly designed PC board with adjacent return planes to all signals and PDNs, properly bonded I/O cable shields, well bonded shielded enclosures with minimal slots or gaps, and common mode filtering on all I/O and power cables for unshielded products is generally required for best EMI performance. Paying attention to these factors early in the design greatly reduces the risk of EMC and EMI compliance failures. These design details will be covered in the next article.

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COMMON COMMERCIAL EMC STANDARDS

►COMMERCIAL STANDARDS

The following are some of the most common commercial EMC standards. Most standards have a fee associated and most on the list are linked back to the source where they're available. If you're purchasing the printed version of this guide, then refer to the Standards Organizations in the References section for standards purchase information. Note that many Euro Norm (EN) versions of IEC standards may be purchased at a considerable discount from the Estonian Centre for Standardization, [https://www.evs.ee.](https://www.evs.ee/Esileht/tabid/111/language/en-US/Default.aspx)

FCC

<https://www.ecfr.gov>

Electronic Code of Federal Regulations (e-CFR) CFR 47 - Part 15 (Radio Frequency Devices)

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ANSI Accredited C63 www.c63.org

Asia Pacific Laboratory Accreditation Cooperation (APLAC) <https://www.apac-accreditation.org/>

BSMI (Taiwan) <http://www.bsmi.gov.tw/wSite/mp?mp=95>

Canadian Standards Association (CSA) www.csa.ca

CISPR [http://www.iec.ch/dyn/www/f?p=103:7:0::::FSP_ORG_](http://www.iec.ch/dyn/www/f?p=103:7:0::::FSP_ORG_ID,FSP_LANG_ID:1298,25) [ID,FSP_LANG_ID:1298,25](http://www.iec.ch/dyn/www/f?p=103:7:0::::FSP_ORG_ID,FSP_LANG_ID:1298,25)

CNCA (China) <https://carbonneutralcities.org/>

Electromagnetic Compatibility Industry Association UK <http://www.emcia.org>

FDA Center for Devices & Radiological Health (CDRH) <https://www.fda.gov/MedicalDevices/default.htm>

Federal Communications Commission (FCC) www.fcc.gov

Federal Standards https://quicksearch.dla.mil/qsSearch.aspx **Gosstandart** (Russia) <https://gosstandart.gov.by/en/>

IEC <https://www.iec.ch/homepage>

IEEE Standards Association <https://standards.ieee.org/>

IEEE EMC Society Standards Development Committee (SDCOM) <https://standards.ieee.org/develop/index.html>

Industry Canada (Certifications and Standards) [http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/h_sf06165.](http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/h_sf06165.html) [html](http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/h_sf06165.html)

ISO (International Organization for Standards) <http://www.iso.org/iso/home.html>

RTCA <https://www.rtca.org>

SAE EMC Standards Committee www.sae.org

SAE EMC Standards [http://www.sae.org/servlets/works/committeeHome.](http://www.sae.org/servlets/works/committeeHome.do?comtID=TEVEES17) [do?comtID=TEVEES17](http://www.sae.org/servlets/works/committeeHome.do?comtID=TEVEES17)

VCCI (Japan, Voluntary Control Council for Interference) http://www.vcci.jp/vcci_e/

COMMON EMC-RELATED EQUATIONS

OHMS LAW

Ohms Law "formula wheel" for calculating resistance (R), voltage (V), current (I) or power (P), given at least two of the other values.

BANDWIDTH VERSUS CLOCK FREQUENCY

 $BW_{Clock}(GHz) = 5 X F_{Clock}(GHz)$

Assuming the rise time of a clock is 7% of the period, we can approximate the bandwidth as shown.

Example, for a clock frequency of 100 MHz, the bandwidth is 500 MHz. That is, the highest significant sinewave frequency component in a clock wave is the fifth harmonic.

PERIOD VERSUS FREQUENCY

$$
F_{Clock}(GHz) = \frac{1}{T_{Clock}(nsec)}
$$

SPEED OF SIGNALS

In air: 12 inches/nsec

In most PC board dielectrics: 6 inches/nsec

VSWR AND RETURN LOSS

RETURN LOSS, GIVEN FORWARD/REVERSE POWER

 $RL(dB) = -10\log(\frac{P_{OUT}}{P_{av}})$

EIRP (EFFECTIVE ISOTROPIC RADIATED POWER)

The antenna transmitted power. Equal to the transmitted output power minus cable loss plus the transmitting antenna gain.

$$
EIRP = P_{out} - C_t + G_t
$$

P_r = P_{out} - C_t + G_t - P_l + G_r - C_r

Where P_{out} = Output power of transmitted in dBm

- C_t = Transmitter cable attenuation in dB
- G_t = Transmitting antenna gain in dBi
- G_r = Receiving antenna gain in dBi
- P_1 = Path loss in dB
- C_r = Receiver cable attenuation in dB
- P_r = Received power level at receiver input in dBm
- P_s = Receiver sensitivity in dBm

RETURN LOSS, GIVEN VSWR

 $RL(dB) = -20\log(\frac{VSWR - 1}{VSWR + 1})$

Return Loss, given reflection coefficient (ρ)

 $RL(dB) = -20log(\rho)$

E-FIELD FROM DIFFERENTIAL-MODE CURRENT

 $\left|{E_{D,max}}\right| = 2.63 * 10^{-14} \frac{|I_D| f^2 Ls}{d}$

ID = differential-mode current in loop (A)

 $f = frequency(Hz)$

 $L =$ length of loop (m)

s = spacing of loop (m)

 d = measurement distance (3 m or 10 m, typ.)

(Assumption that the loop is electrically small and measured over a reflecting surface)

E-FIELD FROM COMMON-MODE CURRENT

 $|E_{c,max}| = 1.257 * 10^{-6} \frac{|I_c| fL}{d}$

IC = common-mode current in wire (A)

 $f = frequency(Hz)$

 $L =$ length of wire (m)

 d = measurement distance (3 m or 10 m, typ.) (Assumption that the wire is electrically short)

ANTENNA (FAR FIELD) RELATIONSHIPS

Gain, dBi to numeric $Gain_{numeric} = 10^{dBi/10}$

Gain, numeric to dBi $dBi = 10\log(Gain_{numeric})$

Gain, dBi-to-Antenna Factor $AF = 20 \log(MHz) - dBi - 29.79$

Antenna Factor-to-gain indBi $dBi = 20 \log(MHz) - AF - 29.79$

Field Strength given watts, numeric gain, distance in meters

$$
V/m = \frac{\sqrt{30 * watts * Gain_{numeric}}}{meters}
$$

Field Strength given watts, dBi gain, distance in meters

 $V/m = \frac{\sqrt{30*watts*10^{(dBi/10)}}}{meters}$

Transmit power required, given desired V/m, antenna numeric gain, distance in meters

$$
Watts = \frac{(V/m * meters)^2}{30 * Gain_{numeric}}
$$

Transmit power required, given desired V/m, antenna dBi gain, distance in meters

$$
Watts = \frac{(V/m * meters)^2}{30 * 10^{4Bl/10}}
$$

PC BOARD

1 oz. copper = 1.4 mils = 0.036 mm

0.5 oz. copper = 0.7 mils = 0.018 mm

Convert mils to mm: multiply by 0.0254 mm/mil

Convert mm to mils: multiply by 39.4 mil/mm

Signal velocity in free space: approx. 12 in/ns

Signal velocity in FR-4: approx. 6 in/ns

WORKING WITH DB

The decibel is always a ratio

Power Gain = $P_{\text{out}}/P_{\text{in}}$

Power Gain(dB) = $10\log(P_{out}/P_{in})$

Voltage Gain(dB) = $20\log(V_{\text{out}}/V_{\text{in}})$

Current Gain(dB) = $20\log(I_{\text{out}}/I_{\text{in}})$

We commonly work with:

dBm (referenced to 1 mW)

dBμV (referenced to 1 μV)

dBμA (referenced to 1 μA)

Power Ratios

10 dB = $10X$ (or $/10$) the power

Voltage/Current Ratios 6 dB = double (or half) the voltage/current

10 dB = triple the voltage or current

20 dB = 10X (or /10) the voltage/current

FIELD STRENGTH EQUATIONS

DBM TO DBUV CHART

DBM, DBμV, DBμA (CONVERSION)

Note: For current relationships, substitute A for V

A common formula for converting default spectrum analyzer amplitudes (dBm) to the limits as shown in the emissions standards (dBµV):

dBm to dB μ V, use: dB μ V = dBm + 107

WAVELENGTH EQUATIONS (FREE SPACE)

Wavelength(m) = 300/f(MHz) Half wavelength(ft.) = 468/f(MHz)

RESONANCE OF STRUCTURES

Use this handy chart for determining the resonant frequency versus cable or slot length in free space. Half-wavelength slots or cables simulate dipole antennas and are particularly troublesome.

DIPOLE RADIATION VERSUS LENGTH

Use this chart to for determining the relative radiation versus size in wavelength. Image Source: Bruce Archambeault.

For example, a wire or slot whose length is 0.2 wavelength at a particular frequency, would radiate about 15 dB down from the equivalent half-wavelength wire or slot.

GAIN OF A HALF-WAVE DIPOLE ABOVE AN ISOTROPIC ANTENNA GAIN - G_{dBi}: G_{dBi} = 10*log(G_r) = 10*log(1.64) = 2.15 dB

VOLTAGE AND POWER RECEIVED BY A HALF-WAVE DIPOLE:

(Assumes receiver input impedence is 50 Ohms)

 $V(\mu V) = E(\mu V/m) * 39.4667/f(MHz)$

W(dBm) = -90 + 10*log[V² (µV)/50]

LINKEDIN GROUPS

[Electromagnetic Compatibility Forum](https://www.linkedin.com/groups/3772603/) [Electromagnetics and Spectrum Engineering Group](https://www.linkedin.com/groups/48713/) [EMC - Electromagnetic Compatibility](https://www.linkedin.com/groups/3106840/) [EMC Experts](https://www.linkedin.com/groups/1784463/) [EMC Troubleshooters](https://www.linkedin.com/groups/6583636/)

[ESD Experts](https://www.linkedin.com/groups/881257/) [Signal & Power Integrity Community](https://www.linkedin.com/groups/8429851/) [EMI/EMC Testing](https://www.linkedin.com/groups/6574381/) [iNARTE](https://www.linkedin.com/groups/7001556/) [IEEE](https://www.linkedin.com/groups/3188262/)

COMMON SYMBOLS

Ref: ANSI/IEEE 100-1984, IEEE Standard Dictionary of Electrical and Electronics Terms, 1984.

ACRONYMS

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RECOMMENDED EMC BOOKS, MAGAZINES AND JOURNALS

ITEM 2023

(Interference Technology Engineer's Master)

ITEM is an exhaustive guide full of invaluable EMC directories, standards, formulas, calculators, lists, and "how-to" articles, compiled in easy-to-find formats. <https://learn.interferencetechnology.com/item-2023/>

2023 EMC Fundamentals Guide

The Fundamentals Guide keeps your project running smoothly by better understanding how to address EMI and EMC in the early design phases.

[https://learn.interferencetechnology.com/2023-emc](https://learn.interferencetechnology.com/2023-emc-fundamentals-guide/)[fundamentals-guide/](https://learn.interferencetechnology.com/2023-emc-fundamentals-guide/)

2020 Europe EMC Guide

This guide features technical articles, reference materials, a company directory, and a products and services list for more than 10 countries.

[https://learn.interferencetechnology.com/2020-europe](https://learn.interferencetechnology.com/2020-europe-emc-guide/)[emc-guide/](https://learn.interferencetechnology.com/2020-europe-emc-guide/)

2019 Components & Materials Guide

This guide is updated with the most critical changes in standards, upcoming events, new product distributors, and more as they relate to EMI shielding and filtering. [https://learn.interferencetechnology.com/2019](https://learn.interferencetechnology.com/2019-components-and-materials-guide/) [components-and-materials-guide/](https://learn.interferencetechnology.com/2019-components-and-materials-guide/)

André and Wyatt,

EMI Troubleshooting Cookbook for Product Designers SciTech Publishing, 2014. Includes chapters on product design and EMC theory & measurement. A major part of the content includes how to troubleshoot and mitigate all common EMC test failures.

Archambeault,

PCB Design for Real-World EMI Control Kluwer Academic Publishers, 2002.

Armstrong,

EMC Design Techniques For Electronic Engineers

Armstrong/Nutwood Publications, 2010. A comprehensive treatment of EMC theory and practical product design and measurement applications.

Armstrong,

EMC For Printed Circuit Boards - Basic and Advanced Design and Layout Techniques

Armstrong/Nutwood Publications, 2010. A comprehensive treatment of PC board layout for EMC compliance.

ARRL,

The RFI Handbook

(3rd edition), 2010. Good practical book on radio frequency interference with mitigation techniques. Some EMC theory.

Bogatin,

Signal & Power Integrity - Simplified

Prentice-Hall, 2009 (2nd Edition). Great coverage of signal and power integrity from a fields viewpoint.

Brander, et al,

Trilogy of Magnetics - Design Guide for EMI Filter Design, SMPS & RF Circuits

Würth Electronik, 2010. A comprehensive compilation of valuable design information and examples of filter, switch-mode power supply, and RF circuit design.

Goedbloed,

Electromagnetic Compatibility

Prentice-Hall, 1990. Good general text on EMC with practical experiments. May be out of print.

Kimmel and Gerke,

Electromagnetic Compatibility in Medical Equipment IEEE Press, 1995. Good general product design information.

Mardiguian,

Controlling Radiated Emissions by Design

Springer, 2016. Good content on product design for compliance.

Kunkel,

Shielding of Electromagnetic Waves, Theory and Practice Springer. 2019. Provides efficient ways for design engineers to apply electromagnetic theory in shielding of electrical and electronic equipment.

Hall, Hall, and McCall,

High-Speed Digital System Design - A Handbook of Interconnect Theory and Design Practices Wiley, 2000.

Joffe and Lock,

Grounds For Grounding

Wiley, 2010. This huge book includes way more topics on product design than the title suggests. Covers all aspects of grounding and shielding for products, systems, and facilities.

RECOMMENDED EMC BOOKS, MAGAZINES AND JOURNALS

Johnson and Graham,

High-Speed Digital Design - A Handbook of Black Magic Prentice-Hall, 1993. Practical coverage of high speed digital signals and measurement.

Johnson and Graham,

High-Speed Signal Propagation - Advanced Black Magic Prentice-Hall, 2003. Practical coverage of high speed digital signals and measurement.

Ott,

Electromagnetic Compatibility Engineering Wiley, 2009. The "bible" on EMC measurement, theory, and product design.

Paul,

Introduction to Electromagnetic Compatibility Wiley, 2006 (2nd Edition). The one source to go to for an upper-level course on EMC theory.

Mardiguian,

EMI Troubleshooting Techniques McGraw-Hill, 2000. Good coverage of EMI troubleshooting.

Montrose,

EMC Made Simple

Montrose Compliance Services, 2014. The content includes several important areas of EMC theory and product design, troubleshooting, and measurement.

Morrison,

Digital Circuit Boards - Mach 1 GHz Wiley, 2012. Important concepts of designing high frequency circuit boards from a fields viewpoint.

Morrison,

Grounding And Shielding - Circuits and Interference Wiley, 2016 (6th Edition). The classic text on grounding and shielding with up to date content on how RF energy flows through circuit boards.

Sandler,

Power Integrity - Measuring, Optimizing, and Troubleshooting Power Related Parameters in Electronics Systems McGraw-Hill, 2014. The latest information on measurement and design of power distribution networks and how the network affects stability and EMC.

Slattery and Skinner,

Platform Interference in Wireless Systems - Models, Measurement, and Mitigation

Newnes Press, 2008. The first publication to publicize the issue of self-interference to on-board wireless systems.

Smith,

High Frequency Measurements and Noise in Electronic **Circuits**

Springer, 1993. A classic book on high frequency measurements, probing techniques, and EMC troubleshooting measurements.

Smith and Bogatin,

Principles of Power Integrity for PDN Design - Simplified Prentice-Hall, 2017. Getting the power distribution network (PDN) design right is the key to reducing EMI.

Williams,

EMC For Product Designers

Newnes, 2017. Completely updated text on product design for EMC compliance.

Weston,

Electromagnetic Compatibility - Methods, Analysis, Circuits, and Measurement

CRC Press, 2017 (3rd Edition). A comprehensive text, encompassing both commercial and military EMC.

Witte,

Spectrum and Network Measurements

(2nd edition), SciTech Publishing, 2014. The best text around explaining the theory and usage of spectrum and network analyzers.

Wyatt and Jost,

Electromagnetic Compatibility (EMC) Pocket Guide SciTech Publishing, 2013. A handy pocket-sized reference guide to EMC.

Wyatt and Gruber,

Radio Frequency (RFI) Pocket Guide

SciTech Publishing, 2015. A handy pocket-sized reference guide to radio frequency interference.

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