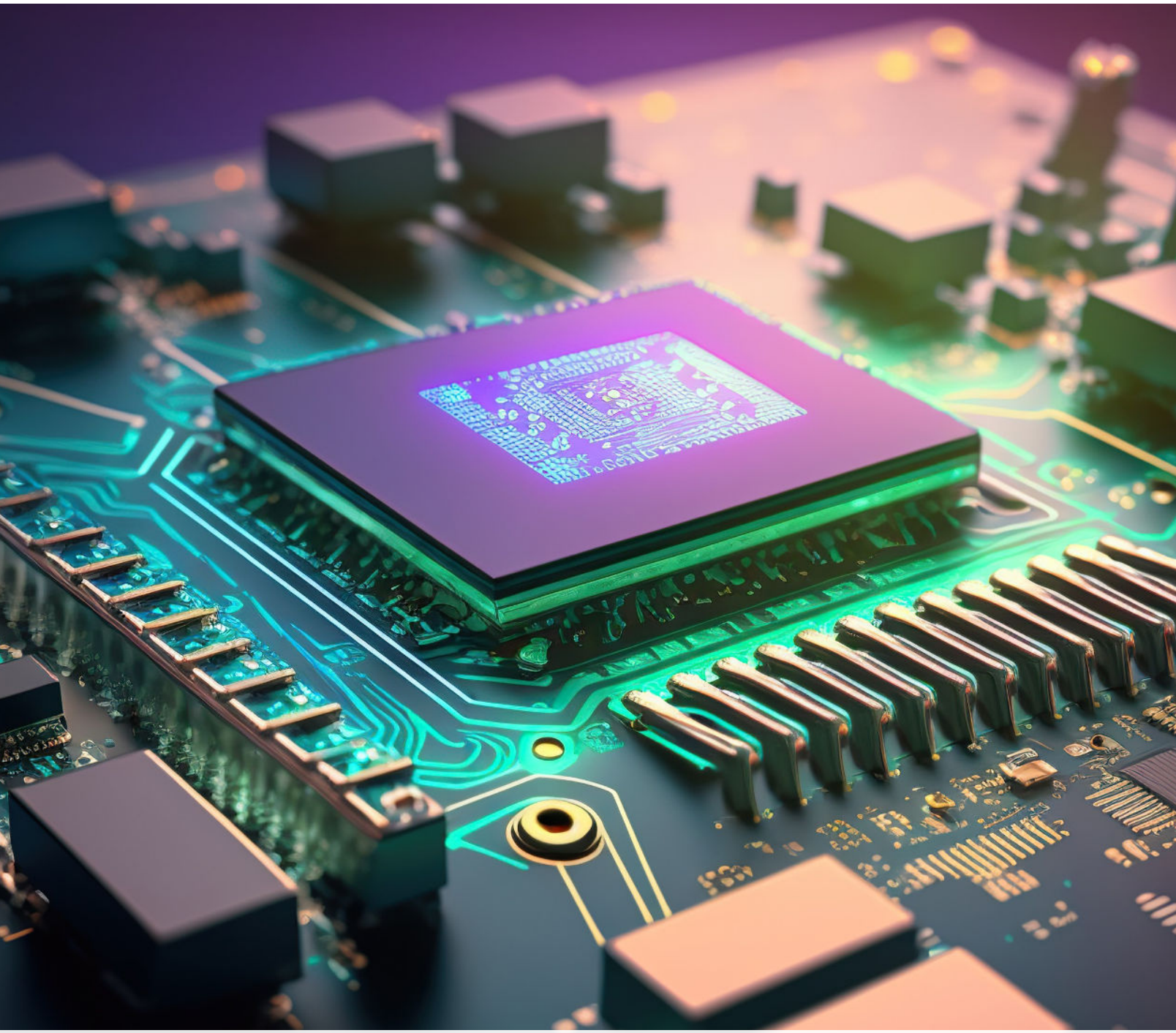
PRESENTED BY

INTERFERENCE TECHNOLOGY®

2023 SIGNAL & POWER INTEGRITY GUIDE

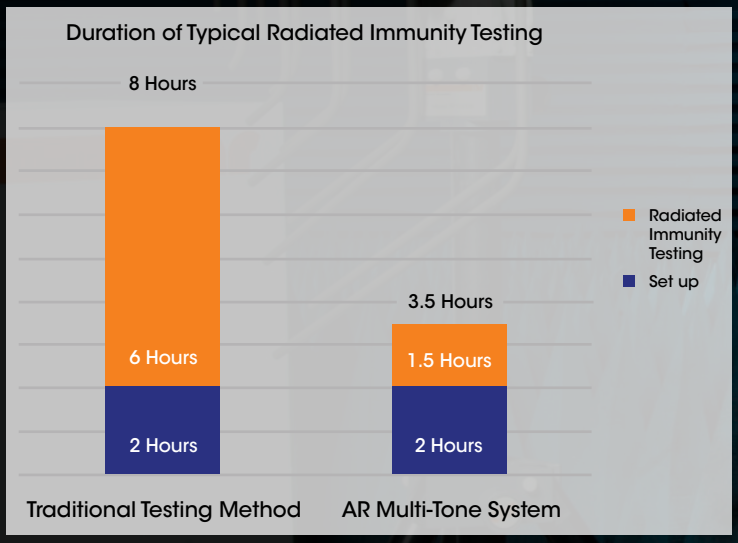


INTERFERENCE TECHNOLOGY GUIDE SERIES | interferencetechnology.com

This is How You Reduce Testing Time by More Than 50%

With regulatory adoption of multiple signal radiated immunity test methods (IEC-61000-4-3:2020, 4th edition), AR's Multi-Tone System enables you to vastly reduce your test times in accordance with automotive, commercial, and aviation EMC RI standards. Included is AR's proprietary emcware® software, offering users numerous test and calibration routines utilizing multiple signal methodology, to meet these standards.

For example, AR's Multi-Tone System can reduce the typical time to run traditional tests such as IEC 61000-4-3, ISO 11451, and ISO 11452, by over 50%. In the event of an EUT failure, margin investigation and traditional single tone testing is easily performed through AR's emcware® software.



Multiple full sweeps are often required during mitigation efforts, which is where the multiple signal approach will pay dividends.

This is a creative way to help your company be more profitable by using your assets more efficiently.

Visit us at www.arworld.us or call 215-723-8181. Talk to an applications engineer at 800.933.8181.

TABLE OF CONTENTS

TECHNICAL EDITORIAL BOARD MEMBERS

Meet the 2023 Editorial Board

GHERY PETTIT | PRESIDENT, PETTIT EMC CONSULTING LLC

Ghery S. Pettit received the BSEE degree from Washington State University in 1975. He has worked in the areas of TEMPEST and EMC for the past 47 years. Employers were the US Navy, Martin Marietta Denver Aerospace, Tandem Computers and Intel Corporation, prior to retiring from industry in 2015 and becoming an independent consultant.

Mr. Pettit is presently serving as Chair of CISPR SC I and is one of CISPR's representatives on the Advisory Council on EMC (ACEC) within the IEC. He has been involved in CISPR activities since 1998, both as a member of the US Technical Advisory Groups to CISPR SC G and CISPR SC I and as an active member of CISPR SC I and its maintenance teams, CISPR SC I MT7 (CISPR 32 maintenance) and CISPR SC I MT8 (CISPR 35 maintenance). He is also a member of the working groups preparing the next editions of ANSI C63.4, C63.9 and C63.16.

ZACHARIAH PETERSON | NORTHWEST ENGINEERING SOLUTIONS

Zachariah Peterson received multiple degrees in physics from Southern Oregon University and Portland State University, and he received his MBA from Adams State University. In 2011, he began teaching at Portland State University while working towards his Ph.D. in Applied Physics. His research work originally focused on topics in random lasers, electromagnetics in random materials, metal oxide semiconductors, sensors, and select topics in laser physics; he has also published over a dozen peer reviewed papers and proceedings. Following his time in academia, he began working in the PCB industry as a designer and technical content creator. As a designer, his experience focuses on high-speed digital systems and RF systems for commercial and mil-aero applications. His company also produces technical content for major CAD vendors and consults on technology strategies for these clients. In total, he has produced over 2,000 technical articles on PCB design, manufacturing, simulation, modeling, and analysis. Most recently, he began working as CTO of Thintronics, an innovative PCB materials startup focusing on high-speed, high-density systems.

He is a member of IEEE Photonics Society, IEEE Electronics Packaging Society, American Physical Society, and the Printed Circuit Engineering Association (PCEA). He previously served as a voting member on the INCITS Quantum Computing Technical Advisory Committee working on technical standards for quantum computing and quantum electronics. He now sits on the IEEE P3186 Working Group focused on Port Interface Representing Photonic Signals Using SPICE-class Circuit Simulators.

TECHNICAL EDITORIAL BOARD MEMBERS

Meet the 2023 Editorial Board

MIKE VIOLETTE | iNARTE CERTIFIED EMC ENGINEER

Mike is President of Washington Laboratories and Director of American Certification Body. He has over 35 years of experience in the field of EMC evaluation and product approvals and has overseen the development of engineering services companies in the US, Europe and Asia. Mike is currently on the Board of Directors of the IEEE EMC Society.

He is a Professional Engineer, registered in the State of Virginia. He has given numerous presentations on compliance topics and is a regular contributor to technical and trade magazines.

DAVID A. WESTON | iNARTE EMC ENGINEER

David A. Weston is an electromagnetic compatibility (EMC) consultant and certified National Association of Radio and Telecommunications Engineers (iNARTE) EMC engineer at EMC Consulting Inc. Merrickville, Ontario, Canada. A life member of the Institute of Electrical and Electronics Engineers, Weston has worked in electronic design for 55 years, specializing in the control, prediction, measurements, problem solving, analysis, and design aspects of EMC for the last 44 years.

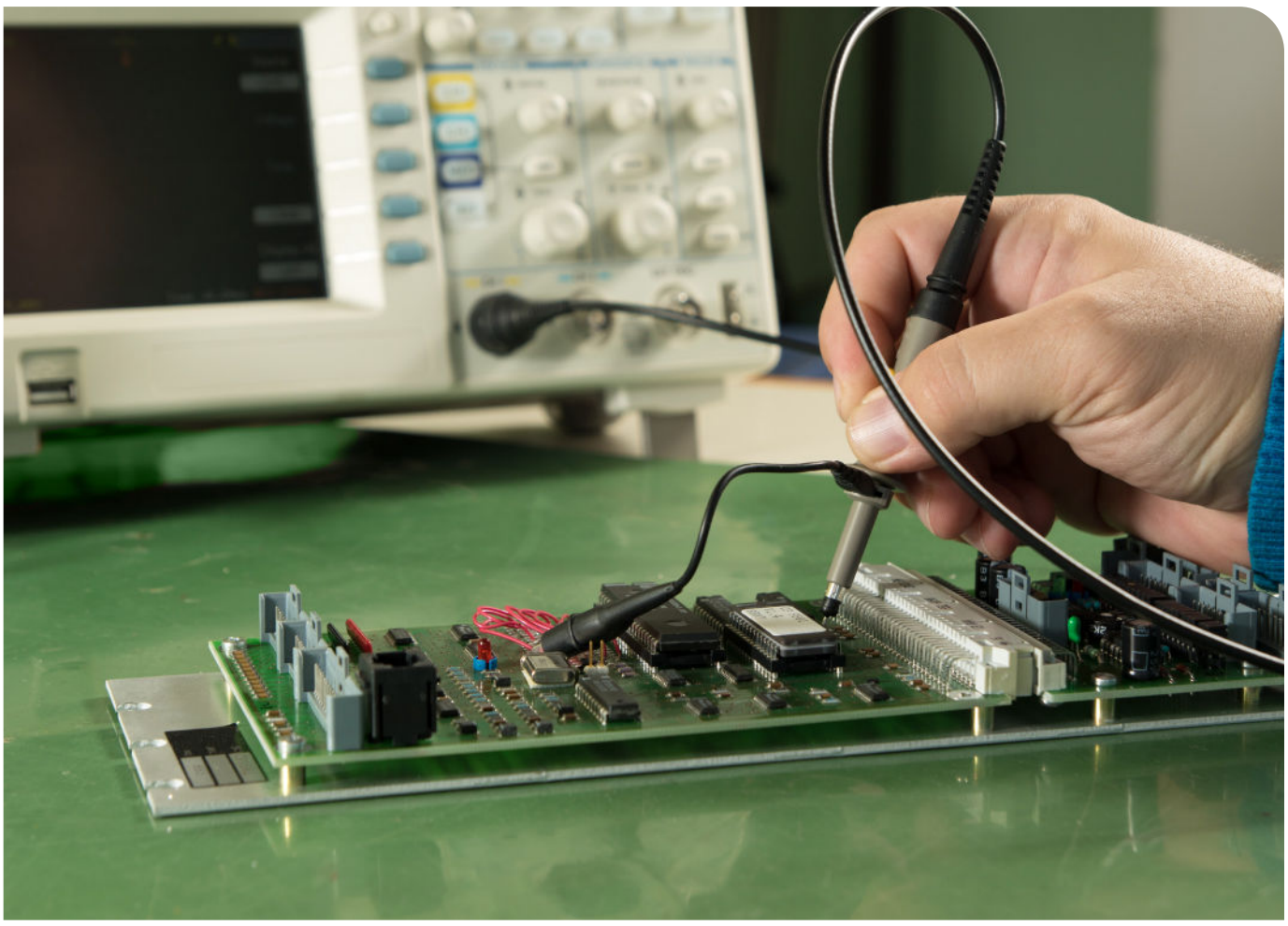
He is the author of the third edition of the 1,157-page book Electromagnetic Compatibility, Methods, Analysis, Circuits, and Measurement published by CRC press in 2017, as well as numerous papers of a practical nature.

TOP THREE EMI AND POWER INTEGRITY PROBLEMS WITH ON-BOARD DC-DC CONVERTERS AND LDO REGULATORS

Kenneth Wyatt
Wyatt Technical Services LLC

Steve Sandler
Picotest Systems, Inc.

Modern devices are continuing a long-term trend of squeezing more electronics into smaller packages, while also increasing system performance, data rates and operating efficiency. Higher efficiencies are often achieved by implementing faster silicon MOSFETs or even faster eGaN FETs while size is reduced by increasing switching frequencies and replacing aluminum and tantalum capacitors with smaller ceramic devices. One result of this trend is that there is greater interaction between the disciplines of EMI, signal integrity (SI) and power integrity (PI).



INTRODUCTION

EMI is a measure of the electromagnetic emissions produced by the high-speed current and voltage signals the system creates. Power integrity is a measure of the power quality at the device that being powered. This means that the power supply voltages must be maintained within the allowable operating voltage range of high-speed devices.

Devices, such as modems, reference clocks and low noise amplifiers (LNAs) are all sensitive to noise on the power rails, which results in timing jitter, spurious responses reduced data channel eye openings, and degraded signal-to-noise ratio (SNR). This too, is a measure of power integrity.

The power supply itself is a noise source and the noise sources generated by the power supply must be kept from propagating through the system.

This article discusses the three most common causes of EMI and power integrity issues while providing tips for how to avoid or minimizes them in your design,

1. **Ringing** on switched waveforms causes broad resonant peaks in the emission spectrum.
2. **DC-DC converters generate noise** at the switching frequency, and because of high speed switching devices, can generate broadband switching harmonics well into the GHz.
3. **Power plane resonance** in DC-DC converter or LDO regulators due to high-Q capacitors resonating with power planes.

RINGING AND RADIATED EMISSIONS

Any ringing on the switched waveform (fairly common) can lead to broadband resonances in the resulting RF spectrum. Resonant frequencies resulting from DC-DC converters or low dropout (LDO) linear regulators can be as low as a few kHz while resonance due to the PDN with switching devices, such as MOSFET's can be in hundreds of MHz or higher.

The harmonic energy resulting from this switching is "captured" by the PDN and device resonances, evident as ringing in the time domain. The current and voltage of this ringing produces EMI. The magnitudes of the ringing and EMI are related to the quality factor (Q) and characteristic impedance of the resonance and the harmonic energy produced by the switching.

As an example, the switching waveform on a DC-DC buck converter demo board was measured with a Rohde & Schwarz RTE 1104 oscilloscope and Rohde & Schwarz RT-ZS20 1.5 GHz active probe (*Figure 1*).

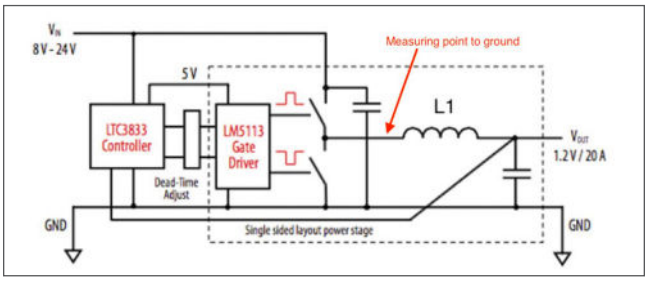


Figure 1. Diagram showing the measuring point at the switch device junction (on the left side of L1) to ground return.

There was a very large ringing superimposed on the switched waveform of 216 MHz. This can be seen clearly in *Figure 2*.

A Fischer Custom Communications F-33-1 current probe was used to measure both the input power cable common mode current (violet trace) and output load differential mode current (aqua trace). See *Figure 3*. Note the broad resonant peaks at 216 MHz (*marker 1*) and the second harmonic at 438 MHz (*marker 2*).

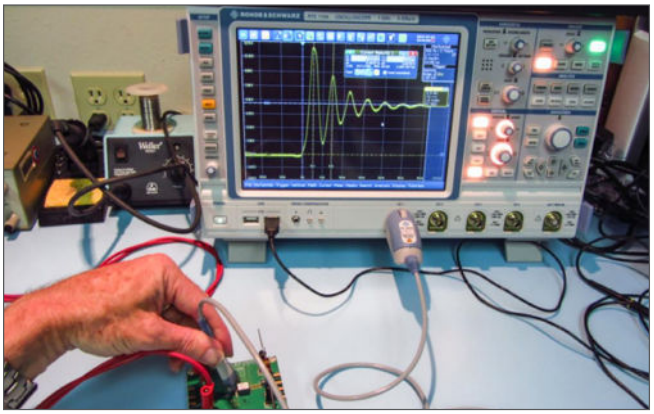


Figure 2. Measuring the rise time and ringing on a DC-DC converter. Notice to strong ringing at 216 MHz.

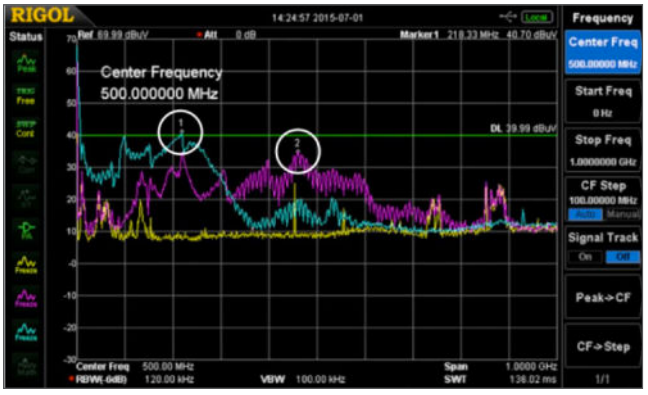


Figure 3. Resulting resonances from the 216 MHz ring frequency (marker 1) and second harmonic at 438 MHz (marker 2).

Remediation Tips - There are several ways to improve the design to minimize the resonances, ringing and therefore EMI. Since the energy is related to the switching frequency, rise time of the switching, characteristic impedance, and Q of the resonances, these factors are also the paths to mitigation.

- Slower edges will degrade operating efficiency but reduce high frequency energy
- Careful PCB design and capacitor selection will minimize the characteristic impedance and Q
- Keep traces short and wide and dielectrics thin.
- Keep all the switching circuitry on one side of the board, preferably with a thin dielectric to the respective ground return plane.
- Use of a snubber circuit, damping of resonances using controlled ESR capacitors, or redesign of the inductor for lower leakage inductance.

For additional detail on measuring ringing refer to *Reference 1*.

FAST EDGES CREATE BROADBAND NOISE AT GHz FREQUENCIES

Today's on-board DC-DC converters use switching frequencies as high as 3 MHz. This is an advantage because it allows for physically smaller inductor and filter components, as well as increased efficiency. However, the fast edge speeds create broadband harmonic energy. The bandwidth of this harmonic energy is related to the voltage and current rise time. A 1ns edge speed can produce harmonic energy up to 3 GHz, or more.

These broadband harmonics are the cause of radiated emissions failures and also can affect the receiver sensitivity of any on-board telephone modems or other wireless systems, such as GPS. *Figure 4* shows how a typical DC-DC converter circuit can be characterized using an H-field probe connected to a spectrum analyzer.

It's also possible to connect the probe to an oscilloscope and hold it near each DC-DC converter to get some idea of the ringing, if any, without disturbing the circuit.

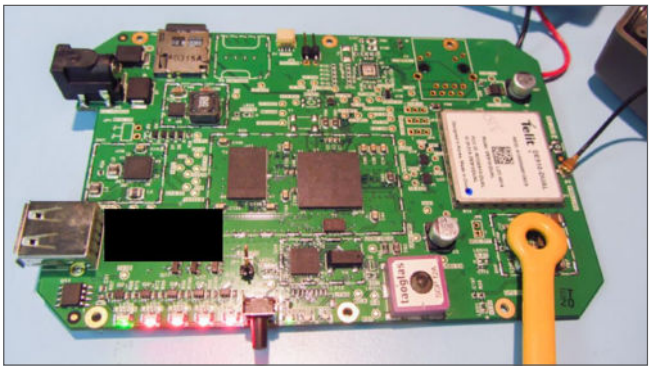


Figure 4. Probing DC-DC converter noise sources on a typical wireless device.

Figure 5 shows the resulting measurement of a couple DC-DC converters. The yellow trace is the ambient noise floor of the measurement system and is always a good idea to record for reference. The aqua and violet traces are the two converter measurements. Note that both produce broadband noise currents out to 1 GHz, with the convertor in violet out to beyond 1.5 GHz. Note the violet trace is 20 to 50 dB higher than the ambient noise floor.

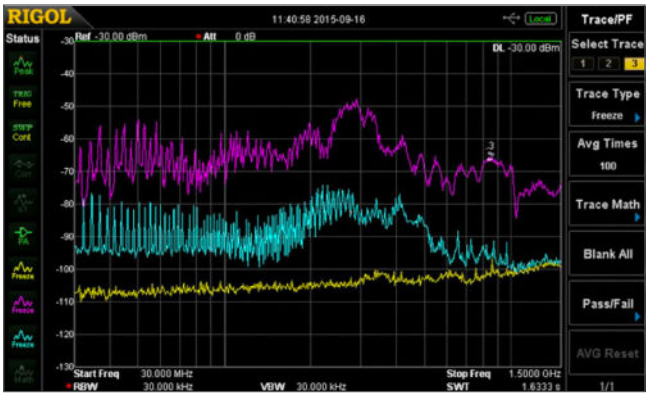


Figure 5. In this example, we're looking from 30 MHz to 1.5 GHz to generally characterize the spectral emissions profile of a couple of on-board DC-DC converters. Both will potentially cause interference to mobile phone bands in the 700 to 950 MHz region. The one with the violet trace is over 30 dB above the ambient noise level in the mobile phone band.

Remediation Tips – To reduce the risk of self-interference to on-board mobile phone modems and wireless systems, the product design must start off with EMC in mind and with no corners cut.

This will consist of:

- A near perfect PC board layout
- Filtering of DC-DC converters
- Filtering of any high frequency device
- Filtering of the radio module
- Local shielding around high noise areas
- Possibly shielding the entire product
- Proper antenna placement

The PC board layout is critical and is where most of your effort should reside. An eight or ten layer stack-up will provide the most flexibility in segregating the power supply, analog, digital, and radio sections and provide multiple ground return planes, which may be stitched together around the board edge to form a Faraday cage. Care must be taken to avoid return current contamination between sections – especially in the ground return planes. For wireless products, the power plane for the radio modem section should be isolated (except via a narrow bridge) from the digital power plane. All traces to this isolated plane should pass over the bridge connecting the two. This can provide up to 40 dB of isolation between the digital circuitry and radio.

It is vital that the power and ground return planes be on adjacent layers and ideally 3-4 mils apart at the most. This will provide the best high frequency bypassing. All signal layers should be adjacent to at least one solid ground return plane. Clock, or other high-speed traces, should avoid passing through vias and should not change reference planes.

Power supply sections should be well isolated from sensitive analog or radio circuitry (including antennas). Be aware of primary and secondary current loops and their return currents. These return currents should not share the same return plane paths as digital, analog, or radio circuits. Remember that high frequency return currents want to return to the source directly under the source trace.

For more details on resolving DC-DC converter noise issues with wireless radio modems, refer to *Reference 2.*

PC BOARD PLANE RESONANCE AND THE EFFECT ON RADIATED EMISSIONS

Noise propagation in a simple system can be represented by three elements, the voltage regulator, the printed circuit board planes with decoupling capacitors (PDN) and the device being powered (load).

Each of these three elements is comprised of resistive, inductive and capacitive terms. Even “noise free” low dropout (LDO) regulators can be highly inductive (*Reference 3*). The resistive, inductive and capacitive terms can resonate amplifying the noise signals created by the power supply and the load as they travel across the PDN creating EMI. The harmonics of the switching frequency and the switch ringing discussed earlier excite these PDN resonances (*Reference 4*). As stated previously this noise can degrade and interfere with on-board wireless modems, as well as resulting radiated and conducted emissions.

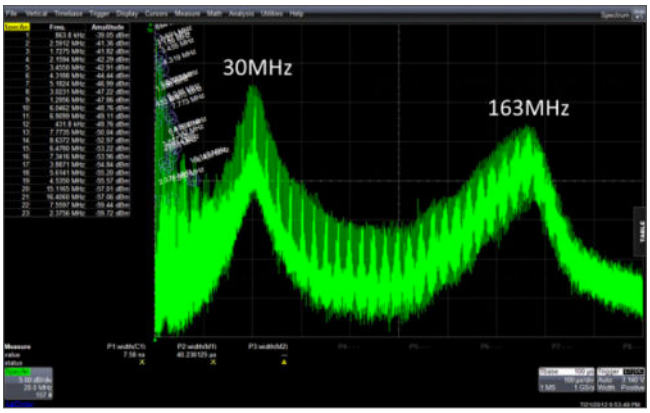


Figure 6. Spectrum analyzer display showing the 30 MHz and 160 MHz resonances detected near the input power connections of a DC-DC converter.

A short video helps explain the basic principles of PDN design (*Reference 5*). The radiated EMI of a LTC3880 DC-DC converter measured near the input plane using an H-field probe is seen in *Figure 6*.

The 163 MHz is attributed to the ringing of the switches as seen in *Figure 7*. This ringing is caused by the inductance of the upper MOSFET bond wires, pins and circuit board planes, ringing with the lower MOSFET and PC board capacitance.

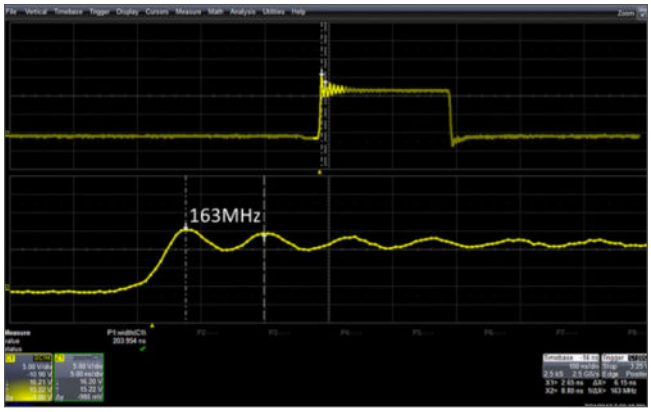


Figure 7. The 163 MHz EMI is easily explained by the ringing at the switch device, as discussed earlier.

The input ceramic decoupling capacitor resonates at approximately 30 MHz, as seen in *Figure 8* and results in the large 30 MHz EMI signature.

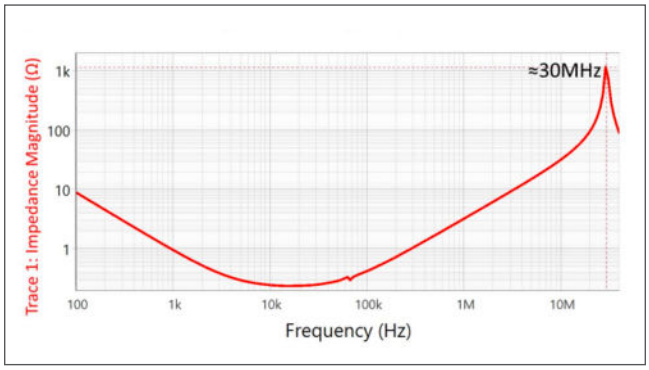


Figure 8. The larger 30 MHz emission is identified as a printed circuit board resonance using an H-field probe and confirmed by a 1-port reflection impedance measurement at the input capacitor.

The input power plane section of the DC-DC converter (measured in *Figure 6*) is shown in *Figure 9* with schematic representations of the component, PC board and external connections.

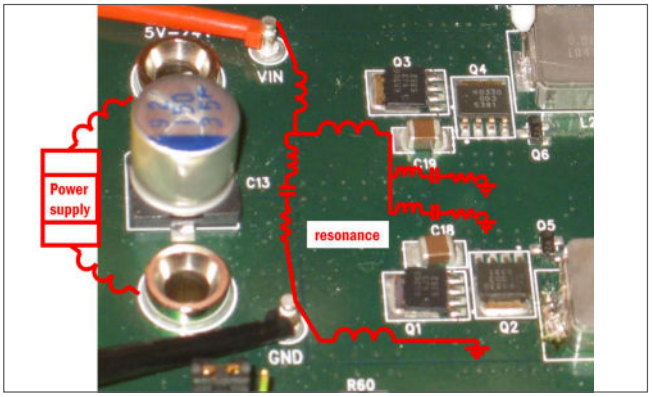


Figure 9. The power plane section of the DC-DC converter (measured in Figure 6) with schematic representations of the component, PC board and external connections.

A very simple simulation example can be used to illustrate these impedance resonance effects. Consider a simple DC-DC converter as shown in *Figure 10*.

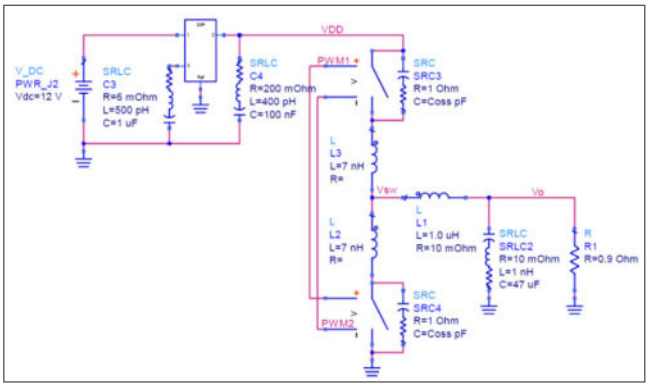


Figure 10. A simple DC-DC converter for illustration of plane resonance EMI. The "FET" switches include lead inductance and drain capacitance (Coss). A small PC board and two ceramic capacitors are included.

Designers frequently place the FET switches on one side of the board with power entry on the opposite side of the PC board. The small PC board plane used in this example has power entry through a pair of pins and no interconnect inductance is added to connect power to the PC board. A large 47 µF ceramic capacitor is placed on the top side of the PC board, while a smaller, 0.1 µF ceramic capacitor is placed very close to the FET switches on the bottom side of the PC board. Two parallel vias connect power and ground from the top side of the PC board to the bottom side as seen in *Figure 11*.

The simple model is used to simulate the harmonic current in the input connector, which is directly related to conducted and radiated emissions. Two simulations are performed; one with low ESR ceramic capacitors and the other with a lower Q controlled ESR ceramic replacing the 0.1 µF capacitor close to the FET switches. Both simulations are shown together in *Figure 12*.

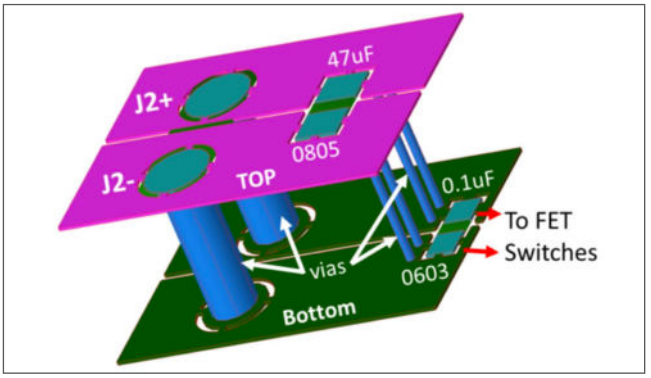


Figure 11. The large round pins on the left are the input power connector, J2. The larger capacitor on the top side is an 0805 sized 47 µF and the smaller capacitor on the bottom side is an 0603 sized 0.1 µF.

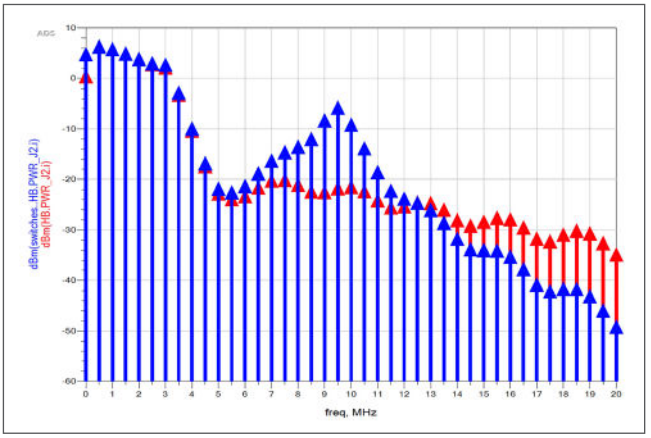


Figure 12. Spectral simulation of the input power lead shows the high Q ceramic (10 mΩ blue) has a clear peak near 10 MHz that is eliminated using a controlled ESR ceramic (200 mΩ red)

The simulated impedance, measured at the smaller capacitor in *Figure 13* shows the corresponding plane resonance with a clear 10 MHz peak using the high Q ceramic capacitor (blue) and the peak is eliminated using the controller ESR ceramic capacitor (red).

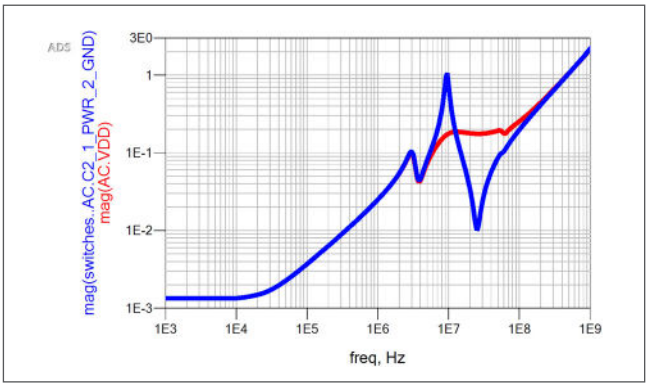


Figure 13. The simulated impedance at the 0.1 uF capacitor using high Q ceramic (10 mΩ blue) and a controlled ESR ceramic (200 mΩ red)

Remediation Tips – To minimize PDN resonances, the complete system of voltage regulator, PDN and the load need to be carefully balanced. Damping resistance must be included to eliminate or minimize the existence or Q of resonances. This will consist of:

- Short, wide power planes
- Keep the layout as small as possible to minimize inductance
- Thinner PC board dielectric layers, closer to the surface
- Incorporate EM simulation to identify and minimize PDN resonances
- Keep capacitors on one side of the PC board to the extent possible
- Low-Q or ESR controlled capacitors reduce Q
- Choose voltage regulators and output capacitors for good control loop stability
- Don't place cutouts or holes in ground plane layers below the power plane
- Ferrite beads are a very common cause of PDN resonances
- Be aware of inductive interconnects bringing power to the system.

Printed circuit board design and decoupling is critical and "rules-of-thumb" generally don't work well in high speed circuits. The design of the circuit board and capacitor decoupling always involves trade-offs, but the impacts on resonances need to be weighed carefully. A multi-frequency harmonic comb generator can be extremely helpful for quickly identifying PDN resonances (*Reference 3*).

SUMMARY

As you can see, designing DC-DC converters, LDOs, and PDNs with today's high-speed technology nearly always requires careful circuit design, adequate filtering, simulation of the PDN, very careful circuit board layout, and use of controlled-ESR filter capacitors. Poor designs can result in:

- Ringing in power supply switches (or other fast-edged digital switching) resulting in associated radiated or conducted emissions resonant peaks at the ring frequency and harmonics.
- High frequency broadband noise well beyond 1 GHz, resulting in self-interference to radio modems.
- Poor stability and resonances in un-damped power distribution networks, leading to instability, spectral resonances, and associated radiated and conducted emissions.

REFERENCES

1. Wyatt, GaN Technology and the Potential for EMI (EDN), http://www.edn.com/electronics-blogs/the-emc-blog/4439839/GaN-technology-and-the-potential-for-EMI
2. Wyatt, Platform Interference (EDN), http://www.edn.com/electronics-blogs/the-emc-blog/4441086/Platform-interference
3. Wyatt, Review: Picotest J2150A Harmonic Comb Generator http://www.edn.com/electronics-blogs/the-emc-blog/4440532/Review--Picotest-J2150A-harmonic-comb-generator
4. Sandler, The Inductive Nature of Voltage Control Loops, http://www.edn.com/electronics-blogs/impedance-measurement-rescues/4438578/The-inductive-nature-of-voltage-control-loops
5. Sandler, How to Design for Power Integrity: Finding Power Delivery Noise Problems (Video), https://www.youtube.com/watch?v=oL6qjhJH_m4&t=4s&list=PLtq84kH8xZ9HIYgBYDsP7TbqBpftidzI8&index=4

POWER INTEGRITY OVERVIEW FOR PCB DESIGNERS

Zachariah Peterson
Owner, Northwest Engineering Solutions LLC

INTRODUCTION

Most PCB designers don't realize they have a power integrity problem until that problem causes a board to fail. Power integrity is also related to two other important areas that repeatedly cause design failures: signal integrity and EMI/EMC. In fact, some common signal integrity problems are related to power integrity in that unstable power leads to signal level and timing fluctuations. In addition, some EMI problems can be caused by excessive emissions by fast transients within a power system.

To help PCB designers and systems engineers better overcome their power integrity problems, it's important first to know how power integrity can cause other problems in a circuit board. This article will give an overview of the power integrity problems more designers are experiencing in modern electronics systems and which will become more prevalent as devices reach greater feature density in the near future.

WHO WORRIES ABOUT POWER INTEGRITY?

Generally, when we refer to power integrity, we refer to AC power integrity, meaning time-varying changes in the power being delivered to a load. DC power integrity is also important, but is more the domain of power electronics rather than high-speed digital systems.

The goal in designing for stable power integrity is to minimize power fluctuations in a PCB as components pull power from the power distribution network (PDN). The typical area where power integrity is important is in boards with many high-speed components, although to an extent the same challenge arises in high-frequency systems. The reason power integrity arises so often in this system is due to the fast edge rates of digital signals; generally any digital system with fast GPIOs, fast SPI buses, and standardized computing peripherals can have power integrity problems.

The result of such power rail and ground plane potential fluctuations includes signal integrity and EMI problems such as:

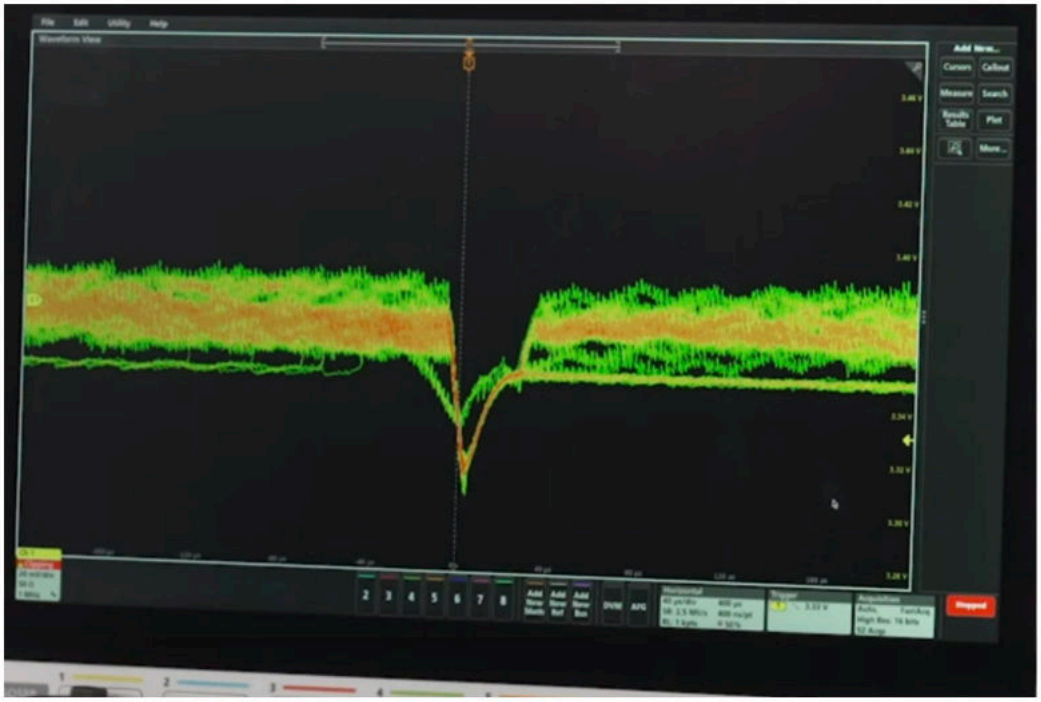
- Transient ringing seen on I/O signal levels
- Jitter, observed in edge transitions in an eye diagram
- Radiated emissions, which may be observed from the surface or board edge
- Noise transfer between poorly isolated rails with the same voltage

These problems can occur despite precise design and layout of power regulator circuits. Of course, power regulators have their own noise challenges, but the noise observed on a power rail in a high-speed PCB is really a low-impedance power delivery challenge, not a regulator noise challenge.

OBSERVING POWER INTEGRITY

The effects of power integrity on power delivery can be measured directly by looking at the voltage provided by a PDN in a PCB. Power is delivered to components by first charging up the capacitance in the PDN; the PDN then discharges some current through the I/O supply when logic outputs switch states. Because modern CMOS-based I/O buffers switch very quickly, they excite a broadband transient in the PDN that exhibits an underdamped oscillation in system voltage level.

Power delivery instabilities can be seen in an oscilloscope trace. The image below shows just such a power droop event occuring at the moment a certain IC switches its logic state with fast edge rate. The resulting voltage dropout in the rail is significant and ends with an underdamped oscillation. If this dropout is too large, it could exceed the lower power limit of components that are drawing power from the PDN, causing system resets.



Significant power droop observed on a 3V3 rail in a single-board computer.

With further probing throughout the PCB, it is possible to identify specific components that may have insufficient decoupling/bypassing and investigate how these are placed in the PCB. The other factor contributing to unstable power delivery is the layer stackup in the PCB. Potential changes to a design can be qualified in simulation to determine their efficacy.

DESIGNING PDN IMPEDANCE

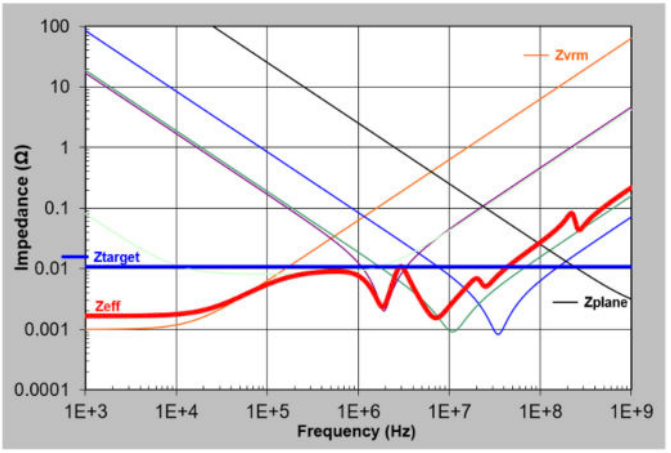
The impedance of the PDN in a PCB is actually a matrix, with its members being self-impedances for each power rail and transfer impedances between power rails. The typical concern in designing the PDN for large processors requiring multiple rails is to ensure the self-impedance for each rail is minimized throughout some relevant bandwidth (typically extending up to GHz frequencies).

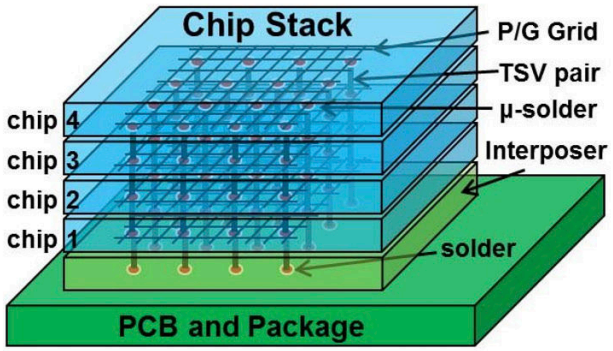
In starting the PDN design process, the designer first needs to formulate two metrics:

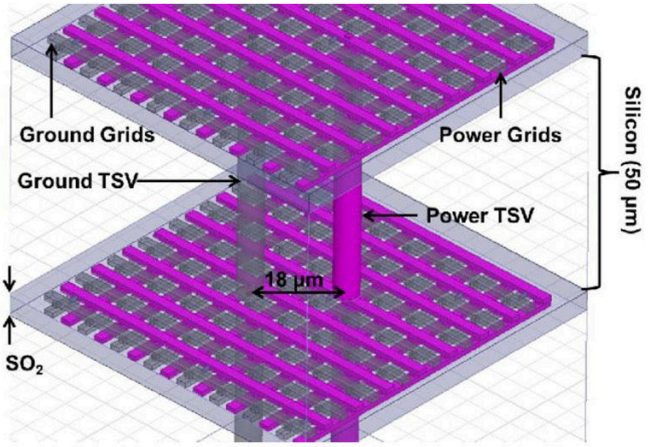
- An acceptable voltage ripple range based on noise margin
- A target impedance based on the expected maximum average current draw and allowed voltage ripple

As core voltages have decreased, being as low as 0.8 V in some components, the noise margin compresses and this creates greater pressure on the PCB designer to ensure lower PDN impedance.

An example PDN impedance spectrum with 1 mΩ target impedance is shown below. In this example, we can see each of the contributors in the PCB layout to the overall impedance (VRM, plane, and groups of decoupling capacitors). This model was generated analytically by considering the equivalent circuit parameters of the structures that make up a PDN in a PCB (planes, vias, traces, capacitor parasitics,VRM model). A more accurate PDN impedance spectrum could be generated using a full-wave solver.







Transfer impedance is used to evaluate isolation between different rails, where the focus is on evaluating how current draw at one port produces a voltage fluctuation at all other ports. This takes a design-simulate-optimize strategy at the circuit level, which can be done in SPICE. This would later be verified in the PCB layout with a full-wave solver, producing an impedance curve similar to the example shown on page 22.

At the system level, we must also consider the on-die PDN impedance, as well as any in-package capacitance used to keep the on-die impedance low. Semiconductor packages can have highly inductive PDN impedance at GHz frequencies, which leads to a large peak (strong antiresonance) in the PDN impedance spectrum. In some cases, the best the PCB designer could do was load up on small-case decoupling capacitors and excess plane capacitance through the stackup design methods shown above.

Modern semiconductor packages, including multi-chip modules and 2.5D/3D integrated packages, could include additional in-package capacitance to ensure lower PDN impedance in the GHz range in order to ensure stable power delivery. An example low-impedance package design methodology involving formation of grounded grids surrounding through-silicon vias in a 3D package is shown above.

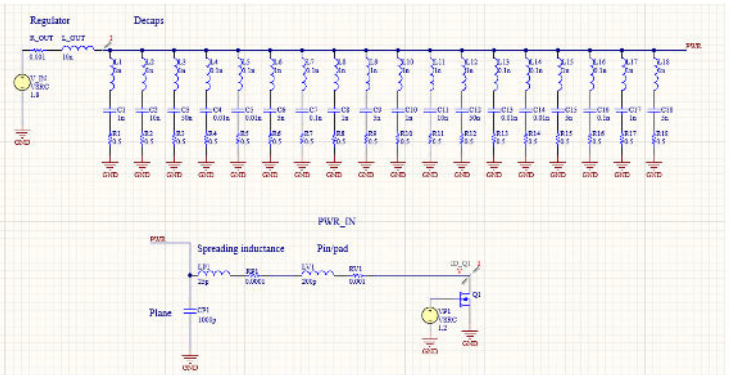
SIMULATING POWER INTEGRITY

The board used to gather the image shown above was built with best practices in terms of its stackup (adjacent power/ground planes), but still the droop arises due to insufficient capacitance in the PDN. These dropout events are difficult to predict during the design phase as they require sophisticated simulations:

- Pre-layout simulations using SPICE-based models
- Post-layout simulations using full-wave electromagnetic field solvers

SPICE-based models have always been phenomenological, although they are effective for evaluating components selection and isolation between power rails. Some of the best EDA vendor tools are now reaching the point where reduced full-wave simulations can be performed directly from PCB layout data to evaluate signal integrity.

The primary quantity to simulate when designing a PCB for stable power integrity is the PDN impedance. This would typically be generated in the frequency domain using S-parameters or transfer functions, or it could be examined in the time domain, where the voltage transient on a power rail is used to determine the PDN's impulse response function. In either case, the goal is to examine the impedance of the PDN given a proposed stackup and known decoupling capacitor counts.



Example SPICE model generated in Altium Designer. This model includes a decoupling capacitor bank, equivalent circuits for planes, and a simple switch to simulate current draw by an integrated circuit.

#	Name	Material	Type	Thickness	Weight	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask	0.8mil		3.5
1	L1 TOP		Signal	1.6mil	1oz	
	Dielectric 1	RO3003 core, 17um rolled copper	Core	5mil		3
2	L2 GND		Signal	0.8mil	1/2oz	
	Dielectric2	RO4450F	Prepreg	5mil		4.2
3	L3 SIGNAL 1		Signal	0.6mil	1/2oz	
	Dielectric3	RO4835 core, 17um "LoPro" copper	Core	10.7mil		3.66
4	L4 GND		Signal	0.6mil	1/2oz	
	Dielectric4	370HR	Prepreg	5mil		4.2
5	L5 SIGNAL 2		Signal	1.2mil	1/2oz	
	Dielectric5	370HR	Core	10mil		4.34
6	L6 SIGNAL 3		Signal	0.6mil	1/2oz	
	Dielectric6	370HR	Prepreg	5mil		4.2
7	L7 GND		Signal	0.8mil	1/2oz	
	Dielectric7	RO3003 core, 17um rolled copper	Core	5mil		3
8	L8 BOTTOM		Signal	1.6mil	1oz	
	Bottom Solder	Solder Resist	Solder Mask	0.8mil		3.5
	Bottom Overlay		Overlay			

This example stackup, generated in Altium Designer, uses hybrid construction to support both high speed digital signals and RF signals. Based on layer thicknesses and Dk values, an ideal place to put a power plane or large power rails would be on L5.

STACKUP AND MATERIALS MATTER

The best predictor of power integrity in a PCB is the design of the stackup. The reason we care about the stackup is because it enables inclusion of plane capacitance through placement of an adjacent power-ground plane pair. Modern processors operating with fast edge rates need to have a power-ground plane pair with high plane capacitance for two reasons:

1. To ensure low PDN impedance up to higher frequencies
2. To compensate for any lack of on-die/in-package capacitance

Ensuring high plane capacitance requires placing the two planes close together on a thin core or prepreg layer, and the separating dielectric must have high dielectric constant. Together, this provides sufficient capacitance and low spreading inductance which can cause the plane's impedance minimum to reach near the GHz range.

To aid power integrity in smaller devices that require significant power draw, some advanced materials vendors supply embedded capacitance materials. These materials are very thin, being designed to separate the power-ground plane pair in the layer stack. They also have high Dk value and high loss tangent in order to provide high capacitance and dampen any radiated emissions from the power-ground plane pair. These materials are used in high layer count rigid or flex PCBs in mobile devices, and in the newer substrate-like PCBs used in modern smartphones.

SUMMARY

As more designers confront power integrity challenges in PCBs and packaging, EDA vendors have a role to play in providing tools to iterate designs without repeated prototyping. The next generation of tools is providing an in-app approach to design optimization without requiring an external simulation program, including in the area of signal and power integrity. As more simulation application vendors form partnerships with EDA/ECAD vendors, we can expect these tool sets to expand to give more designers advanced capabilities for design and simulation in the areas of power integrity, signal integrity, and EMI.

INDEX OF ADVERTISERS

AR RF/Microwave Instrumentation
t: (215) 723-8181
e: info@arworld.us
w: www.arworld.us
page: 2

LECTRIX
t: (484) 688-0300
e: info@lectrixgroup.com
w: www.lectrixgroup.com
page: 17


Break the same old pattern.
Problem First. Product Last.
Strategy | Content | Data | Technology
LECTRIX®
Digital Marketing for the B2B Electronics Industry
1.484.688.0300 | info@lectrixgroup.com
www.lectrixgroup.com