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EMC FILTERS MANUFACTURERS GUIDE

Kenneth Wyatt

Sr. Technical Editor Interference Technology

A Guide to Suppliers of EMI Filters

Your quick reference guide by various EMC filter types. The listing includes AC and DC line filters, filters for chambers, feedthrough, board level, coaxial, ferrite, filtered connectors, power converter, EMP/HEMP, TEMPEST, and *custom. Applications include commercial, military, medical, and industrial. Also includes contact links for suppliers.*

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INPUT FILTERS — THE KEY TO SUCCESSFUL EMC VALIDATION

Ranjith Bramanpalli | Steffen Schulze

Würth Elektronik

Introduction

Input filters are today as ever a requisite factor for successful EMC validation of switching controllers, irrespective of the size of the AC component involved. Switching controllers create conducted EMC interferences due to AC *components in their lines, independent of their individual topology and application. Certain component manufac*turers have therefore optimized their power modules for a low line-bound and radiated emission of interferences. These types of modules' residual ripple generally exhibits a negligibly low value, meaning that an output filter can be dispensed within most applications. Since the input current at the step-down converter is pulsating, this may generate radio-frequency interferences in the application. Depending on the specific application, the hardware developer decides whether an input filter is necessary directly before the power module or in another position in the switch. The design process of input filters for optimized power modules and the measurement techniques that *are used is discussed in this article.*

INPUT FILTERS – THE KEY TO SUCCESSFUL EMC VALIDATION

As a starting point it is useful to illustrate how differential mode noises develop in the first place. Differential mode noises are interference signals in a system with a symmetrical current back and forth between the source and the load in the lines of a switching controller.

Figure 1 – Symmetrical system

In the input circuit, the clock frequency of the power module includes an AC component superimposed over the useful current and is similar in its configuration to the current through the storage inductance of the power module. The input current flows into the input capacitor Cin. Real capacitors possess a resistive component, the ESR, and an inductive component, the ESL as shown in *Figure 2.*

Due to the ESR of the input capacitor and the impedances of the lines of the power module, the AC component produces an undesirable voltage drop.

In this form, the noise voltage shows up as a differential-mode signal. The amplitude of the interference voltage occurring at the input capacitor is essentially dependent on the ESR of the capacitor used. Electrolytic capacitors have a relatively high ESR, the value of which can range between just a few milliohms up to several ohms. As a consequence, the interference voltage can vary between a few millivolts up to several volts. Ceramic capacitors, on the other hand, have a very small ESR of just a few milliohms and thus result in a noise voltage of a few millivolts. In addition, the circuit-board design of the power module exerts a great effect on the interference voltage.

Figure 2 – Development of the noise voltage

To reduce differential mode noises, at least one simple LC filter must be fitted at the input of the converter as a measure to minimize the AC component in the line. In high-impedance systems, such an input filter can theoretically produce a voltage attenuation of 40 dB/decade in the stopband. In practice, a lower degree of attenuation is achieved since the terminating impedances are lowohm in their nature and also because the components themselves exhibit losses. In dimensioning the LC filter a corner frequency f_c is selected that is below the switching frequency f_{sw} of the power module. If the factor is one tenth, theoretically an insertion loss of 40 dB is achieved at the switching frequency at which the highest spectral amplitude occurs.

$$
f_{\rm C} = \frac{f_{\rm SW}}{10} \tag{1}
$$

The corner frequency of an LC filter is generally:

$$
f_{C} = \frac{1}{2\pi \sqrt{L_{f} \cdot C_{f}}}
$$
 (2)

As an example for the calculation of the filter, an inductance of 10 μH is selected and Equation (2) is transformed to:

$$
C_f = \frac{1}{(2\pi \cdot 0.1 \cdot f_{sw})^2 \cdot L_f}
$$
 (3)

In arranging the filter components, as shown in *Figure 3,* the filter capacitor can be positioned on the side of the voltage source or on the input side of the power module. The decisive factor for the attenuation of the pulsating current drawn from the voltage source is the inductance of the filter inductor.

Figure 3 – Arrangement of the components of the input filter

When the quality of the filter resonance is too high, oscillations may occur in the event of changes in the input voltage that must be regulated. The stability criterion that applies here is that the output impedance of the input filter $Z_{\text{\tiny out,filter}}$ within a broad frequency spectrum has to be lower than the input impedance of the power module $Z_{\text{in,converter}}$:

$$
|Z_{\text{out,filter}}| < |Z_{\text{in,converter}}|
$$
 (4)

In addition, the corner frequency f_c of the input filter

should lie far below the crossover frequency f_{∞} of the power module.

$$
f_{c,filter} \ll f_{co,converter} \tag{5}
$$

Figure 4 shows how this is done by placing an attenuating branch parallel to the power module input.

Figure 4 – Attenuation of the input filter

The attenuator reduces the quality of the input filter and consequently its output impedance at the resonance frequency. *Equation (6)* can be applied to calculate the attenuation resistance Rd for a filter quality of Qf=1:

$$
R_d = \sqrt{\frac{L_f}{C_f}}
$$
 (6)

A value that has established itself in practice as an indicator of the capacity of the attenuation capacitor C_{d} is the five-to-ten-fold measure of the filter-capacitor capacitance:

$$
(5 \cdot C_f) < C_d < (10 \cdot C_f) \tag{7}
$$

As an alternative, the filter can be attenuated by selecting an electrolytic capacitor that is switched parallel to the filter output instead of the attenuator. As a rule, the value of the ESR of the electrolyte capacitor is sufficient to attenuate the filter.

SELECTING THE LC FILTER COMPONENTS

Both capacitors and coils show capacitive as well as inductive properties in reality. Filter inductors have their highest filter effect at their self-resonant frequency (SRF). In coils, the SRF is strongly dependent on the inductance and the capacitive coupling between the winding turns. In capacitors, the SRF is strongly dependent on the capacitance and the length of their terminations. When selecting the filter components, it is hence advisable to make sure that the SRF is at the upper end of the frequency range in which the RFI voltage is at its maximum or, respectively, in which the filter is to be active.

The decisive factor for the reduction of the differential-mode noise is the filter inductor, since this is the component that counteracts the rapid rise and drop in the current in the input circuit. *Figure 5* shows the impedance curves of three rod core chokes based on an example of the Würth Electronics WE-SD product family.

Figure 5 – Example of Impedance of one manufacturer's SD rod core chokes

The higher the inductance, the smaller the SRF. It is recommend-ed to select an inductor with an inductance whose numeric value is lower than the capacitance of the filter capacitor. In practice, a filter inductance with a maximum value of 10 μH is selected, since – depending on the design – such an inductance has a self-resonant frequency of approximately 30 MHz.

Exceeding the rated current of the filter inductor may result in damage to the wire winding. Taking the efficiency of the switching controller as a basis, it is possible to calculate the effective input current of the power module using *Equation 8*.

$$
I_{in} = \frac{V_{out} \cdot I_{out}}{V_{in} \cdot \eta}
$$
 (8)

For safety reasons, a larger value should be selected as the rated current of the filter coil.

The filter capacitor may take the form of a liquid electrolyte capacitor, a polymer capacitor, or even a ceramic capacitor. The only aspect that must be considered is that the filter quality at the corner frequency is sufficiently low.

Further measures must be considered when dimensioning a Π filter. In the optimal case, an input filter should be placed as close as possible to the input of the power module. For the case that the in-put filter is placed further away due to geometric circumstances, the traces may act as an antenna between the input filter and the power module at higher frequencies. The trace inductance can, however, also be used together with a ceramic capacitor to establish an additional LC filter with a higher cut-off frequency *(see Figure 6).* Due to its negligibly low ESR, a ceramic capacitor can swiftly short-circuit high-frequency voltages to ground with low impedance.

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Figure 6 – Π input filter

The SRF of the capacitor should roughly lie within the spectrum of the switching frequency of the power module. To illustrate this point, Figure 7 shows impedance curves of Würth Elektronik WCAP-CSGP ceramic capacitors in the 0805 size.

Figure 7 – Impedance of ceramic capacitors

Of the components shown in *Figure 7*, at a clock frequency of 2 MHz, for example, a capacitor with 1 μF would be suitable (resonant frequency marked in red). Even a 100 nF ceramic capacitor (resonant frequency marked in blue), which is used as a blocking capacitor in numerous electronic circuits, would be a suitable candidate at these values; it should be mentioned, however, that com-pared with the 1 μF version the 100 nF capacitor has an ESR higher by a factor of nine.

DIMENSIONING AN OUTPUT FILTER

Some power modules on the market, such as Würth Elektronik Magl³C power modules, exhibit a negligibly low residual ripple at the output, which is why an output filter is not absolutely necessary. For the case that components supplied by the switching controller decouple interference signals via interfaces (e.g. sensor switches, analog switching circuits), it may be necessary to include an output filter to filter the output voltage.

The circuit schematic shown in *Figure 6* images an output filter as an option comparable to that shown here in *Figure 8.* It is not generally possible to make a definitive statement on the necessity for and effectiveness of such an output filter, since this must be dimensioned individually for each specific application. It may be possible to

use an output filter to reduce the residual ripple of the power module to an absolute minimum, or otherwise to suppress undesirable subharmonic oscillations. The filter can be dimensioned as already described. Attenuation of the filter resonance is not necessary in this case.

Figure 8 – Output filter

MEASURING THE NOISE VOLTAGE

The noise voltage is measured according to the basic standard IEC CISPR 16-2-1, which describes the types of the interference variables to be measured, the equipment to be used for the various interfaces, and the measurement set-up for table-top and floor-standing devices. The interferences are evaluated in the frequency range from 9 kHz to 30 MHz. The measuring devices include besides the EMI receiver a variety of line impedance stabilizing networks (LISNs), voltage probes, current clamps and capacitive couplers. In a measurement set-up for table-top devices, as shown in *Figure 9,* the test object (DUT, "device under test") is positioned on a non-conductive table standing on a ground reference plane. The table should be 40 cm in height. In the case that a vertical ground reference plane is also present, the table should be at least 80 cm in height. The LISN must be connected to the ground plane ensuring good conductivity. The DUT itself and any attached cables are to be arranged so that they are 40 cm distant from the ground plane.

Figure 9 – Test set-up for measuring conducted interferences on power-supply lines

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The length of the cable between the DUT and the LISN should not exceed 80 cm. The EMI receiver evaluates the asymmetric noise voltage that is decoupled at the LISN for the separate leads of the cable.

MEASURING THE RADIATED NOISE

The method for measuring the radiated noise above 30 MHz is described in the IEC CISPR16-2-3 basic standard. The measurement environment is generally in the form of an anechoic room with a conductive floor or, at a smaller scale, an anechoic chamber. Here, too, the DUT is positioned on a non-conductive table (for portable or table-top devices, see *Figure 10*) or on the floor. To enable the DUT to revolve on its own axis in its default state during the measurement, it is placed on a turntable. In larger anechoic rooms, the receiving antenna is placed at a distance of 10 m from the DUT and adjusted in its height during the measurement to find the maxi-mum electric field strength at each measurement frequency (peak spectrum). In addition, the orientation of the antenna is altered (horizontal and vertical polarization). In smaller anechoic chambers, the distance between antenna and DUT should be 3 m; since the antenna height needs to be fixed, the height scan is omitted and he floor between the antenna and the DUT must be covered with absorbing material.

Figure 10 – Test set-up for measuring the radiated noise in anechoic rooms or chambers

CASE STUDY – MEASURED NOISE VOLTAGE

The following section describes the measurement of the noise volt-age using a Würth Elektronik Magl³C power module evaluation board fitted with a Variable Step Down Regulator Module (171 020 601) as an example.

Already during the preliminary phase it is possible to measure the AC component at the power module's input using an oscilloscope. By running an analysis within the time domain, the anticipated interference spectrum can be estimated at the start of the work on the design of the filter.

Figure 11 – Time-domain signal with a broadband spectral content

Figure 11 shows an AC component of 80 mV, measured at an in-put voltage of the power module of 7.5 V, an average input current of 1.2 A, and an average load current of 2 A. Switching controllers have the property to show up as a negative differential resistance from the viewpoint of the power supply. The input current rises with decreasing input voltage. For this reason, the noise voltage is measured under "worst case" conditions – minimum input voltage, maximum current.

Figure 12 – Noise voltage without an input filter

The decisive factor in the analysis of this type of noise emission, however, remains the measurement of noise voltage as can be per-formed in an EMC laboratory. *Figure 12* shows the result of a noise voltage measurement without an input filter.

. This power module operates at a clock frequency of 370 kHz. In the interference spectrum, the highest amplitude (red peak: 68 dBμV) can be measured at this frequency. The amplitude density of the noise voltage drops at a rate of approx. 40 dB/decade, meaning that no significant interference level can be seen above the 15th harmonic. Nevertheless, it is only above the 9th harmonic that the interference level is more than 10 dB below the limit for the average detector (dark blue line).

Equation (3) can now be used to calculate a suitable LC

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input filter. Due to the relatively low switching frequency, an inductor with a low SRF and an inductance of 4.7 μH is selected and the filter capacitance is calculated.

$$
C_f = \frac{1}{(2\pi \cdot 0.1 \cdot f_{sw})^2 \cdot L_f}
$$
 (9)

The selected filter capacitor is the one with a little higher capacitance of 10 μF. The maximum input current is calculated using *Equation (8)*.

This calculation requires the efficiency of the evaluation board, which is determined by measurement and in this case has a value of 91%.

$$
I_{\text{in}} = \frac{5 \text{ V} \cdot 2 \text{ A}}{6 \text{ V} \cdot 0.91} = 1.83 \text{ A}
$$
 (10)

On the basis of the calculations of the filter inductance and input current, it is now possible to select an appropriate inductor. Picked for the purpose is an unshielded inductor from the Würth Elektronik PD2 series, size 5820. Figure 13 shows the result of the noise voltage measurement with the matched filter.

Figure 13 – Noise voltage with an input filter

The interference level measured at the 370 kHz switching frequency has a value of 30 dBμV. The levels of all harmonics are lower than 20 dBµV and are thus sufficiently attenuated. The average level at 370 kHz corresponds to the peak level and is 18 dB lower than the average limit of 47 dBμV. In measuring such conducted interferences in the practical context, a signal-to-noise ratio of this dimension is entirely sufficient in order to confirm the conformity of this measurement.

The purpose of the measurement of the noise voltage is to demonstrate the usefulness of an analysis of the interference potential in the time domain; though an analysis in the frequency domain is still indispensable.

Finally, the equations can be used to calculate an attenuating resistance.

$$
R_{d} = \sqrt{\frac{4.7 \,\mu H}{10 \,\mu F}} = 0.686 \,\Omega \tag{11}
$$

The higher the value of the attenuation resistance, the higher the attenuation of the filter resonance. In this case, the next higher resistance of the E12 series of 1 Ω can be selected.

A value of 47 μF is selected for the attenuation capacitor. This may be, for example, a Würth Elektronik eiCap ceramic capacitor of the WCAP-CSGP series.

MEASURING ACCORDING TO IEC CISPR 22

The above measurements were performed according to the IEC CISPR16-2-1 standard, as described in Section 8. The use of a LISN enabled the asymmetric voltage to be decoupled and equated to the asymmetric (common-mode) voltage, which was then compared to the limit, taken from the IEC CISPR 22 standard for devices for private and commercial use (Class B). For power-supply components – and this includes all types of switching controllers – there is no directly applicable EMC standard. The entire application in which the switching controller is used must be assigned to a specific category of devices and then tested according to the corresponding standard applicable for the product or product family. In this case, the product-family standard IEC CISPR 22 for IT installations was taken only with reference to the limits, which are also given in the IEC 61000-6-3 generic standard. The generic standards can be used in cases for which there is no specific standard for the device in question.

SUMMARY

Irrespective of the size of the AC component involved, an input filter is today as ever a requisite factor for a successful EMC validation of a switching controller. Simple-to-apply equations can be used to calculate such an input filter on an individual basis. Taking the impedances of the filter and the switching controller into account in the equations, this enables oscillations to be avoided and also ensures the control stability of the switching controller itself. A targeted selection of the filter components lays the foundations for an optimal design of the filter. Equipped with an appropriate degree of technical skill in EMC testing methods, the hardware developer can design his switch purposefully and, wherever necessary, make any adjustments to the filter himself.

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DOES THE NUMBER OF BYPASS CAPACITORS FOR A CHIP MATTER?

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Introduction

How do you decide on the size of a bypass capacitor (or capacitors) for your project? Do you need multiple capacitors to bypass a specific chip? Are multiple value capacitors important for a given use? Do you subscribe to the old Wife's Tail about having a couple capacitors a couple orders of magnitude different in value in parallel? Here is one take on the subject for you to consider.

Or not…

DOES THE NUMBER OF BYPASS CAPACITORS FOR A CHIP MATTER?

IS A CAPACITOR JUST A CAPACITOR?

When you took a class in basic circuit theory in college the professor introduced various types of circuit elements as if they were perfect devices. A resistor only had resistance. An inductor only had inductance. And, a capacitor only had capacitance. "Neglecting fringe effects…" was probably heard by the student from the professor. And, due to the law of primacy (that which you learn first sticks with you) many engineers go on believing this to be true, much to the delight of EMC engineers and technicians as this mistaken belief keeps us gainfully employed.

While the concept of a pure capacitor is a useful tool, in a real circuit there is also resistance and inductance involved. The resistance comes from the fact that our circuit boards aren't super conductors and the inductance comes from the fact that a circuit has some length and area to it. For this discussion we'll assume (dangerous word, but…) that the resistance is negligible. Not zero, but close enough for government work. The inductance, however is important.

If we have some small, non-zero, inductance in the circuit we can model the capacitor, as installed, as a series circuit consisting of the capacitor and the small value of inductance.

The value of the impedance of both the capacitor and inductor are dependent on the value of the device and frequency. For the inductor (which we will assume to be 3 nH for this example as that is typical for a bypass capacitor circuit on a PWB) this impedace is:

za za zapostani za zapostali za
Zapostani za zapostani za zapost $Z_1(f) = 2πfL$

And for the capacitor this impedance is:

$$
Z_{\rm c}(f) = 1/2\pi fC
$$

As we are looking at a series LC circuit, the total impedance is 2πfL + 1/2πfC.

The self-resonant frequency where to total impedance is zero (if we are neglecting the small value of resistance that actually exists in the circuit) is:

$$
\frac{1}{2\pi\sqrt{(LC)}}
$$

Below the self-resonant frequency the circuit will appear capacitive and above it the circuit will appear inductive.

EXAMPLES

What does this look like as a function of frequency? Let's take a look at a .1 μF capacitor, in series with 3 nH of inductance, starting at 1 MHz and going through 5 GHz.

The self-resonant frequency for this LC circuit is just below 10 MHz, so if we were looking for bypassing to be effective for radiated emissions we might think this capacitor is too large as 30 MHz is above the self-resonance frequency for the circuit. Let's take a look at a smaller capacitor, say 470 pF. What does the impedance of this circuit look like?

Now we've moved the self-resonant frequency up to just above 100 MHz. That looks better. How about making the capacitor an order of magnitude smaller, 47 pF?

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Now the self-resonant frequency is just above 400 MHz. This should be great.

NOT QUITE SO FAST!

How do you decide on the size of a bypass capacitor (or capacitors) for your project? Do you need multiple capacitors to bypass a specific chip? Are multiple value capacitors important for a given use? Do you subscribe to the old Wife's Tail about having a couple capacitors a couple orders of magnitude different in value in parallel? Here is one take on the subject for you to consider.

The red line is the overall impedance of a series LC circuit with a .1 μF capacitor and a 3 nH inductor, the green line is the same with a 470 pF capacitor and the blue line is the same with a 47 pF capacitor. Yes, the self-resonant frequency is higher for the smaller capacitors, but the ultimate impedance is the same once we are a bit above the self-resonant frequency. Remember, above self-resonance the overall circuit is inductive, and the inductance hasn't changed. Also, the impedance of the capacitors goes up as the value goes down for a given frequency. What do we gain by placing a smaller capacitor in parallel with a larger one? Looking at this graph, not much, if anything. What have we lost by adding a second capacitor for each chip? Extra board real estate and decreased reliability, due to the addition of the extra parts.

Now, this example assumes (dangerous word) that adding a second capacitor hasn't added any inductance to the circuit. Let's take this a bit further. In the real world that second capacitor isn't exactly collocated with the first one, so there's a little bit of extra inductance associated with it. Instead of a circuit that looks like this:

We wind up with a circuit that looks like this:

We wind up with a total impedance looking into the bypass circuit of $Z_{L1} + Z_{C1} \mathbb{I}(Z_{L2} + Z_{C2})$

If we place the larger capacitor on the side towards the chip being bypassed, we assume that the values of the capacitors are .1 μF and .001 μF and we assume that the additional inductance, L2, is perhaps .5 nH, we get an impedance curve something like this (in green). If we superimpose the new curve on the original curve (in red) for the large capacitor (.1 μf) we see just what the new bypass circuit might look like. Not much of an improvement (if any), is there? BTW, the little blip in the green curve around 200 MHz seems to be an artifact from the math program. Blowing up the resolution to 10 kHz steps and looking carefully at the graph reveals that this blip is gone.

Now, just for fun, let's reverse the capacitors so the smaller one (.001 μF) is towards the IC and the larger one (.1 μF) is added "outside" the first capacitor. We get a very interesting change to the graph:

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The trace in green is the total impedance of the bypass circuit with the larger capacitor on the side towards the chip being bypassed and the trace in red is the total impedance of the bypass circuit with the smaller capacitor on the side towards the chip. The large "spike" in the overall impedance shows up in this one for the circuit with the smaller capacitor closer to the IC. Also, note that the self-resonant frequency has shifted ever so slightly lower when we reverse the two capacitors. If a harmonic to be suppressed happened to align with the positive going spike (the parallel resonance just below the crossover frequency) there could be serious trouble with emissions.

Given the overall change (and not for the better with the spike in the total impedance) adding a second capacitor that is smaller has virtually no impact if it is placed outboard of the larger capacitor and a potentially negative effect if the smaller capacitor is placed inboard of the larger capacitor. Use a single bypass capacitor.

NOW, HOW BIG SHOULD THAT ONE CAPACITOR BE?

That's the 64 million dollar question (and if you are too young to understand the reference, look it up on Google, it's so old it was a 64 thousand dollar question "back in the day"). There is no one right answer, but keep in mind that a previous employer of the author simply used .1 μF capacitors (or was it .01 μF, I can't remember) everywhere. And it worked fine. What they did not do was use multiple capacitors of different values for each chip. That capacitor does two jobs. First, it serves as a bypass capacitor to minimize emissions, and second, it serves as a local charge reservoir to allow current to be available to the chip when needed. Those big capacitors where the power comes onto the board are simply too far away to help with this. Their whole purpose is to resupply charge to all the bypass capacitors.

CONCLUSION

There have been many in the past who have advocated that two capacitors, a couple orders of magnitude apart in value, should be used to bypass chips to minimize emissions. I hope you see why this isn't a valid idea. The second capacitor doesn't help, and it costs you space on the board and it costs you decreased reliability due to the extra parts. Not to mention the impact it can have on the overall impedance curve. The only place it helps is your capacitor salesman's commission.

Have fun keeping the board designers honest, and don't tell your professors about how their "neglecting fringe effects" statement to sophomore engineering students keeps you employed.

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REVIEW OF THE EMC FILTERS KIT FROM WÜRTH ELEKTRONIK

Arturo Mediano

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2019 COMPONENTS & MATERIALS GUIDE

REVIEW OF THE EMC FILTERS KIT FROM WÜRTH ELEKTRONIK

Some weeks ago I received one unit of the EMC-Filter kit from Würth Elektronik (Order Code: 744998), a very nice and useful kit for industry and academia *(Fig. 1)*.

Figure 1 – The EMC-Filter kit from Würth Elektronik (Order Code: 744998)

If you are interested in filtering conducted emissions, this is a great kit for evaluation of components and topologies in both differential mode (DM) and common mode (CM) emissions.

The kit is specially useful combined with some kind of simulation tool (i.e. LTSPICE) and some frequency response analyzer as Bode100 from Omicron.

GENERAL VIEW

The box is included in a high quality plastic box with the traditional elegant style from the German manufacturer. Inside of the kit you will find *(Fig. 2)*:

Figure 2 – What you will find inside the kit

• Several PCBs offering an easy way to build up a line filter

- X capacitors for DM filtering (line-neutral)
- Y capacitors for CM filtering (line-earth and neutral-earth)
- Common mode chokes for CM filtering
- Resistors for discharging X capacitors as specified by safety rules
- Tweezers
- SMD terminals
- Plastic spacers
- Brochure and documentation

The kit offers the user and easy way to evaluate the best topology for a given application using the Würth components but I think another great possibility is to use the kit to learn about EMC conducted emissions filters.

TOPOLOGY AND COMPONENTS

The integrated PCBs with different topopologies and footprints for components offer a simple way to try any design in a few minutes.

The basic topology implemented in the PCB boards is in *Fig. 3*:

Figure 3 – Basic topology in the kit.

As a general information for you, in my kit I found basically (this information is orientative and can change in future kits because I know designers in Würth Elektronik are always looking for better and new kits including new components for evaluation:

 • 10 PC boards ready for soldering components using several footprints and combinations.

- Several X2 capacitors with 10nF, 15nF, and 150nF values and rated 275VAC. They will offer a low impedance path to high frequency signals trying to circulate in the LINE-NEUTRAL path.
- 10 resistors with 10Mohm values for discharging the X caps as mandatory from safety regulations. The resistors are connected in parallel with the capacitors.
- A good number of X1/Y2 capacitors with 680pF, 1nF, and 2.2nF values and rated 250VAC They will offer a low impedance path to high frequency signals trying to circulate in the DM (LINE-NEUTRAL) and CM (LINE-EARTH and NEUTRAL-EARTH) path modes.
- Several common mode chokes with 700uH, 1mH, 2.2mH, 3.3mH, 5mH, 6.8mH, 7mH, 9mH, 10mH, 20mH, and 27mH values. The chokes with 7mH and 9mH values are nanocrystalline technology. The CM chokes are used for filtering high frequency signals trying to circulate in the LINE-EARTH and NEU-TRAL-EARTH paths (CM) offering a high impedance to those signals. In theory this component is transparent to the DM signals but, because of the leakage inductance, we will be able to offer some filtering effect with the CX capacitors for differential mode signals.

USING THE KIT AND EXAMPLE

As soon as the kit was in my hands I tried one of the combinations. The process was easy: just choose your components and solder them in the PCB. No detailed analysis (to do later) but a fast working prototype that create enthusiasm for the topic.

I decided to select one 150nF X capacitor, two 1nF Y capacitors, and one 5mH CM choke.

The response of the filter in DM and CM modes was measured with my Bode 100 instrument as shown in *Fig. 4.*

Figure 4 – The DM and CM responses in my first prototype.

Note we can identify the attenuation at different frequencies in both modes, check for parasitic resonances because components and/or layout, and discover underdamping responses that can create special increase in emissions at some frequencies (e.g. 30-40kHz in DM mode). The experience was really positive so, I recommend you to try the kit for your future EMC conduced emissions problems.

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T-FILTERS, TRANSMISSION LINES AND EMC

Aziz Yuldashev *EMC Engineer* [aziz.yulda@gmail.com](mailto:aziz.yulda%40gmail.com?subject=)

Introduction

Have you ever had a signal integrity issue that did not have its toll on EMC? If you did then you should consider *yourself lucky to have avoided this nightmare.*

2019 COMPONENTS & MATERIALS GUIDE

T-FILTERS, TRANSMISSION LINES AND EMC

I. SITUATION:

An I2S bus master clock driver is set to 12.288MHz and run at 3.3V. Drive strength is at 50-Ohms. Rise time is at 2ns. Fall time is at 2ns.

Figure 1 – The Master Clock of I2S Bus

However, hiding behind this promising picture is EMC performance. *Figure 2* shows the Radiated Emissions(RE) of this clock.

Figure 2 – Radiated Emissions of I2S Bus Master Clock

Three spikes shown in *Figure 2* are at 135MHz, 160MHz, and 184MHz. In other words, the 11th, 13th, and 15th harmonic of the master clock radiating through the flex cable were causing emissions failures. To address this issue, the EMC design engineer had placed a T-Filter (Murata NFL18ST506H1A3D) at the input of the flex cable connector on the "Master Board". This filter has a cut-off frequency of 50MHz. As shown in *Figure 3*, the implementation of the filter had a dramatic effect on RE.

Figure 3 – Radiated Emissions of I2S Bus Master Clock with T-Filter

Figure 3 is quite good to look at. Having a 5dB margin is a luxury in the EMC world. However, the joy of a 5dB margin did not last long. When the master clock line was re-analyzed for Signal Integrity (SI), well, *Figure 4* was the result.

Figure 4 – Signal Integrity of the Master Clock with T-Filter Implemented

Adding the T-Filter to the transmission line added 110pF of capacitance to ground resulting in a reflection caused by a phase shift. Due to this reflection the VOL margin was lost and introduced a concern of false edge detection.

II. SOLUTIONS CONSIDERED WITHOUT THE USE OF FILTERS:

Note: The design team rejected all proposals for layout changes because of procedural and requirement constraints. Other solutions needed to be considered.

Reducing the drive strength

Increasing the rise and fall times can mask reflections, but not always. This solution would work if the transmission line was not 14 inches long. Reducing drive strength worked great for EMC, but resulted in cut-off transmission.

Reducing the line voltage

The master clock was run at 3.3V, however the I2S bus can operate at 1.8V without any issues. Luckily there was a place holder for a level shifter (SN74AUP1T34) implemented on the PCB whose pads were populated with zero-ohm resistors. Implementing the level-shifter to drop the line voltage from 3.3V to 1.8V resulted in SI similar to *Figure 1* and RE performance similar to *Figure 3*.

III. AVOIDING THIS TYPE OF A PROBLEM:

Shorten the Transmission Line

The distance traveled by the transmission line between the I2S driver and the receiver should be as short as possible. Ideal situation for a bus traveling from the "master board" to the "slave board" is to place the driver and the receiver close to the connectors leaving/entering boards. In the example discussed if the trace length on the "slave board" was very short then placing the T-Filter may not have caused the signal integrity problem.

Properly Match Impedances

If the length of the transmission line is constricted due to some design constraints then it is important to make sure there is no mismatch at the source and load of the transmission line. One could consider a series match or a parallel match schemes *(refer to Chapter 4 of Introduction to Electromagnetic Compatibility, 2006 by Clayton R. Paul).*

Avoid Vias

We have seen cases where transmission lines cross board layers though vias. When cross-sectional dimensions of the transmission line change, the characteristic impedance of the line will change and will create a reflection at that discontinuity. A signal passing through a via will encounter a discontinuity.

SI Budgeting

It is important to determine the signal integrity budget of the transmission line. This can be done at the layout stage of the design. Using the Cadence/Allegro/Spice tools the margin/bandwidth-for-error can be calculated by adding capacitance, inductance and DCR to the transmission line. For instance, doing this will let you know how much added capacitance (due to filters, between traces, between connectors, etc.) you could tolerate on the transmission line and still have good SI.

IV. SUMMARY

The layout of the transmission lines must be properly implemented following good design practices for SI. Having good signal integrity provides margin/bandwidth for implementing EMC fixes (if there is any), such as placing a T-Filter (or any other means of filtering) without distorting the signal significantly. Finally, it is always a good idea to have an EMC engineer review your board layout before building the board.

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LINKEDIN GROUPS

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- <u>。</u>Audience Development

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THE IMPORTANCE OF LAYOUT IN ESD SUPPRESSING DIODES

Aziz Yuldashev *EMC Engineer* [ndemyanovich@leadertechinc.com](mailto:ndemyanovich%40leadertechinc.com%20?subject=)

THE IMPORTANCE OF LAYOUT IN ESD SUPPRESSING DIODES

ESD protection of sensitive electronics via transient voltage suppression (TVS) diodes is becoming a common circuit technique across industries. Signal lines in a circuit that are accessible to humans by touch (such as USB, HDMI, etc.) require ESD protection on all sensitive signal lines that are input to some IC's. Placement of the ESD protection diodes on the circuit board relative the IC's they are protecting play a significant role. It is important to understand the behavior of PCB traces of signals at transient conditions such as ESD. As an example, a simple schematic of an I2C bus extender with TVS diodes is shown in *Figure 1.*

Figure 1 – Common schematic of TVS protection devices.

The realistic model of this circuit at transient ESD is shown in *Figure 2.*

Figure 2 – A realistic model of common schematic showing trace inductances and parasitic capacitances.

PCB traces will have inductances associated with them based on their length. Consider the SDA signal trace. Trace lengths connecting the following points are very important:

- The trace length from node A to the cathode of the diode.
- The trace length from the anode of the diode to the ground connection.

• The trace length from node A to the input pin of the IC.

In other words, the ESD protection diode must be placed as close to the pin that it is protecting as possible and its connection to the reference plane must be made as close to the anode pin as possible. Otherwise the trace inductance between any of these points may be large enough that due to the input capacitance of the IC and the stray capacitance of the trace, a tank circuit may form. The tank circuit may oscillate at voltages that can exceed the input voltage capability of the IC and can cause substantial damage to the IC.

This scenario was modeled in LTSpice. *Figure 3* shows the schematic created in LTSpice. It consists of two parts. The first part is the Human body model for ESD based on IEC 61000-4-2 test method. The second part is the representation of *Figure 2* for trace SDA. The *Figure 3* representation is for a diode (10Vclamp) that was placed properly with very short traces at all points listed above, thus resulting in very small trace inductances. *Figure 4* shows the voltage at the CMOS based input (represented by a capacitor).

Figure 3 – LTSpice ESD circuit model for a properly-placed diode.

Figure 4 – Voltage at the CMOS based input for a properly-placed diode.

When the ESD protection diode is placed properly by having the shortest possible traces, the ESD pulse is clamped down by the diode to a safe level. This diode and its placement work well to protect the IC from ESD.

On the other hand, *Figure 5* shows a schematic for a diode (10Vclamp) that was not placed properly. The trace from node A to the cathode of the diode in *Figure 2* is about 1 inch long and was estimated to be about 1 nH. The trace from anode to ground is about 0.03 inches and was estimated to be about 250 pH. *Figure 6* shows the voltage at the CMOS based input (represented by a capacitor).

Figure 5 – LTSpice ESD Circuit Model for Improperly Placed Diode

Figure 6 – Voltage at the CMOS based input for an improperly-placed diode.

Figure 6 clearly shows the effect of long traces connecting the diode cathode to the node of the signal line and the diode anode to the ground. The oscillation observed peaks at 21V and rings at the frequency dictated by the trace inductance, stray capacitance of the line and the input capacitance of the IC.

CONCLUSION

To minimize oscillations on I/O lines due to ESD and to avoid IC damage, the following must be assured:

- Clamping (TVS) diode must be placed as close to the IC pin as possible.
- The trace leading to the cathode of the diode must be as short as possible.
- The trace leading to ground return from the anode of the diode must be as short as possible.

GALVANIC CHART

Mike Oliver, VP Electrical Engineering MAJR Products Corp.

INTERFERENCE TECHNOLOGY

Cathotic metals - least suseptable to corrosion (noble to less noble - vertical to horizontal) Anodic metals - most suseptable to corrosion (less noble to noble - horizontal to vertical)

Green - Metals in harsh or marine environments such as salt spray or salt water. Volt potential difference equal or less than 0.15V

Blue - Metals in normal environments without temperature or humidity control, warehouse storage. Volt potential difference equal or less than 0.45V Yellow - Metals in controlled environments with temperature and humidity control. Volt potential difference equal or less than 0.95V

Red - Not recommended

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- 3. Ott, *Electronic Compatibility Engineering*, Wiley, 2009. A good general purpose text on EMC design, including shielding.
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LINKEDIN GROUPS

- Electromagnetic Compatibility Forum
- EMC Electromagnetic Compatibility
- **EMC Experts**
- **EMC Testing and Compliance**
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