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# FUNDAMENTALS GUIDE



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# INTRODUCTION

# **Kenneth Wyatt**

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Electromagnetic compatibility (EMC) and the related electromagnetic interference (EMI) seems to be one of those necessary evils that must be overcome prior to marketing commercial or consumer electronic products, as well as military and aerospace equipment. Unfortunately, few universities and colleges teach this important information, with the result that products are rarely designed to meet EMC/EMI requirements. EMC or EMI compliance is often left to the end of a project with all the associated schedule delays and unplanned cost.

The purpose of this short guide is to help product designers or EMC engineers learn enough of the basics of EMC and EMI so that the usual design failures are addressed early, when costs and design is minimized. Achieving EMC/EMI is easy once the basics are understood. The content has been updated with the latest information and two new articles have been added - one on ESD design and the other featuring special issues with DC-DC power converters.

Today, with all the myriad of electronic products, including wireless and mobile devices, compatibility between devices is becoming even more important. Products must not interfere with one another (radiated or conducted emissions) and they must be designed to be immune to external energy sources. Most countries now impose some sort of EMC standards to which products must be tested.

# **Basic Definitions**

Let's start with some basic definitions, and there's a subtle difference. EMC implies that the equipment being developed is compatible within the expected operating environment. For example, a ruggedized satellite communications system when mounted in a military vehicle must work as expected, even in the vicinity of other high-powered transmitters or radars. This implies both emissions and immunity in close environments. This usually applies to military and aerospace products and systems, as well as automotive environments.

EMI, on the other hand, is more concerned with one product interfering with existing radio, television, or other communications systems, such as mobile telephone. It also includes immunity to external energy, such as electrostatic discharge and power line transients. This usually applies to commercial, consumer, industrial, medical, and scientific products.

# **Why Do Products Radiate or are Susceptible?**

So, why do electronic products radiate or are susceptible to external energy sources? It's all about controlling the energy from internal sources from coupling out causing interference and external energy sources (ESD, etc.) from getting into and disrupting sensitive circuitry.

For example, the most common issue for most products is radiated emission. We have an energy source, and somehow, this energy source couples harmonic currents to an "antenna-like structure", such as an I/O cable. See *Figure 1*.



Figure 1 - A simple model for radiated emissions. Take away any of the three elements and you have no EMI.

Internal energy sources might include high frequency clocks or any high speed, fast-edged digital signal. These may be transferred via conduction, radiation, inductive, or capacitive coupling mechanisms. For example, a common situation is harmonics of a fast-edged clock (say an Ethernet clock) coupling to an I/O cable, which acts as an antenna and radiates. If these harmonic emissions are over certain limits, the product fails the compliance test and must be redesigned to reduce or eliminate the coupling.

The reverse is also common. A good example is external ESD energy coupling to a poorly shielded or terminated I/O cable and allowing the resulting high transient current to disrupt (or destroy) sensitive circuitry.

The three top product failures I see all the time as a consultant are (1) radiated emissions, (2) radiated susceptibility, and (3) electrostatic discharge. In many cases, these failures are due to poorly-designed PC boards. We'll discuss these and more in this EMC Fundamentals Guide.

We'll start off with some very basic EMC theory, describe some common product design issues, and wrap up with a host of additional reference material, such as lists of common EMC standards, additional reference articles, books, and many other charts and tools.

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# EMC EQUIPMENT MANUFACTURERS

# **Introduction**

*The following chart is a quick reference guide of test equipment and includes everything you'll need from the bare minimum required for key evaluation testing, probing, and troubleshooting, to setting up a full in-house pre-compliance or full compliance test lab. The list includes ampliers, antennas, current probes, ESD simulators,*  LISNs, near field probes, RF signal generators, spectrum analyzers, EMI receivers, and TEM cells. Equipment rental *companies are also listed. The products listed can help you evaluate radiated and conducted emissions, radiated*  and conducted immunity and a host of other immunity tests, such as ESD and EFT.







# BASIC EMI CONCEPTS

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# BASIC EMI CONCEPTS

Understanding EMC is all about two important concepts: (1) all currents flow in loops and (2) high frequency signals are propagated as electromagnetic waves in transmission lines and the field energy travels through the dielectric. The two concepts are related because they are intertwined together. Digital signals create the propagating field, which induces the convection current to flow in the copper traces/planes.

# **CURRENTS FLOW IN LOOPS**

These two concepts are closely related and coupled to one another. The problem we circuit designers miss is defining the return path back to the source. If you think about it, we don't even draw these return paths on the schematic diagram - just showing it as a series of various "ground" symbols.

So what is "high frequency"? Basically, anything higher than 50 to 100 kHz. For frequencies less than this, the return current will tend to follow the shortest path back to the source (path of least resistance). For frequencies above this, the return current tends to follow directly under the signal trace and back to the source (path of least impedance).

Where some board designs go wrong is when high *dV/ dt* return signals, such as those from low frequency DC-DC switch mode converters or high di/dt return signals get comingled with I/O circuit return currents or sensitive analog return currents. We'll discuss PC board design in the next article. Just be aware of the importance of designing defined signal and power supply return paths. That's why the use of solid return planes under high frequency signals and then segregating digital, power, and analog circuitry (keeping them separate) on your board is so important.

# **HOW SIGNALS MOVE**

At frequencies greater than DC, digital signals start to propagate as electromagnetic

waves in transmission lines. As shown in *Figure 1*, a high frequency signal propagates along a microstrip transmission line (circuit trace over return plane, for example), and the wave front induces a conduction current in the copper trace and back along the return plane. Of course, this conduction current cannot flow through the PC board dielectric, but the charge at the wave front repels a like charge on the return plane, which "appears" as if current is flowing. This is the same principle for capacitors and Maxwell called this effect "displacement current".

The signal's wave front travels at some fraction of the speed of light, as determined by the dielectric constant of the material, while the conduction current is comprised of a high density of free electrons moving at about 1 cm/

second. The actual physical mechanism of near light speed propagation is due to a "kink" in the E-field, which propagates along the molecules of copper. Refer to *References 1, 2,* and *3* for further details.



Figure 1 - A digital signal propagating along a microstrip with currents shown.

The important thing is that this combination of conduction and displacement current must have an uninterrupted path back to the source. If it is interrupted in any way, the propagating electromagnetic wave will "leak" all around inside the PC board dielectric layers and cause electromagnetic coupling and "common mode" currents to form, which then couple to other signals (cross-coupling) or to "antenna-like structures", such as I/O cables or slots/apertures in shielded enclosures.

Most of us were taught the "circuit theory" point of view and it is important when we visualize how return currents want to flow back to the source. However, we also need to consider the fact that the energy of the signal is not only the current flow, but an electromagnetic wave front moving through the dielectric, or a "field theory" point of view. Keeping these two concepts in mind just reinforces the importance of designing transmission lines (power and signal traces with return path directly adjacent), rather than just simple circuit trace routing.

It is very important to note that all power distribution networks (PDNs) and high frequency signal traces are transmission lines and the energy is transferred as electromagnetic waves at about half the speed of light in normal FR4-type board dielectrics. We'll show what happens when the return path or return plane is interrupted by a gap in the next article. More on PDN design may be found in *Reference 4, 5*, and *6*.

# **DIFFERENTIAL MODE VERSUS COMMON MODE CURRENTS**

Referring to *Figure 2*, the differential mode current (in blue) is the digital signal itself (in this case, shown in a ribbon cable). As described above, the conduction current and associated return current flow simultaneously as the signal wave front moves along the transmission line formed by the microstrip and return plane.

The common mode current (in red) is a little more complex in that it may be generated in a number of ways. In the fig-

ure, the impedance of the return plane results in small voltage drops due to multiple simultaneous switching noise (SSN) by the ICs. These voltage drops induce common noise currents to flow all over the return (or reference) plane and hence, couple into the various signal traces.



Figure 2 - An example of differential and common mode currents.

Besides SSN, common mode currents can also be created by gaps in return planes, poorly terminated cable shields, or unbalanced transmission line geometry. The problem is that these harmonic currents tend to escape out along the outside of shielded I/O or power cables and radiate. These currents can be very small, on the order of μA. It takes just 5 to 8 μA of current to fail the FCC class B test limit.

# **SUMMARY**

To summarize product design for EMI compliance, a properly designed PC board with adjacent return planes to all signals and PDNs, properly bonded I/O cable shields, well bonded shielded enclosures with minimal slots or gaps, and common mode filtering on all I/O and power cables for unshielded products is generally required for best EMI performance. Paying attention to these factors early in the design greatly reduces the risk of EMC and EMI compliance failures.

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![](_page_10_Picture_3.jpeg)

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![](_page_10_Picture_5.jpeg)

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# DESIGN FOR COMPLIANCE ESSENTIALS

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## *Introduction*

*While unrealistic to discuss all aspects of product design in a single article, I'll try to describe the most common design*  issues I find in the hundreds of client products I've had a chance to work on. These issues generally include PC board design, cables, shielding, and filtering. More detailed information may be found in the Reference section below.

*As previously mentioned, the top three product failures I run into include (1) radiated emissions, (2) radiated susceptibility, and (3) electrostatic discharge. Other failures can include things like conducted emissions, electrically fast*  transient, conducted susceptibility, and electrical surge. Most of these last items are also the result of the same poor *product designs, which cause the top three failures.*

*NOTE: I prefer to avoid the word "ground" in this article or in my consulting practice. The reason is that there are too many misinterpretations,*  which can also lead to EMC failures. It's much more clear to use power and power return, and signal and signal return - or just "return plane" or reference plane. Finally, cable shields or shielded enclosures are "bonded" together - not "grounded". The only exception is the so called "safety ground" or earth ground. But these have nothing at all to do with proper EMC design - just personal safety against electrical shock. I suppose the one exception would be the earth ground connection on a three-wire power line filter. Also, occasionally, there will be an earth ground on a PC board - especially for power supplies, but again, connecting a product or system to earth ground will not improve EMI, due to the very high *inductance (length) of the wire.*

![](_page_11_Picture_6.jpeg)

# DESIGN FOR COMPLIANCE ESSENTIALS

# **PC BOARD DESIGN**

The single most important factor in achieving EMC/EMI compliance revolves around the printed circuit board design. It's important to note that not all information sources (books, magazine articles, or manufacturer's application notes) are correct when it

comes to designing PC boards for EMC compliance - especially sources older than 10 years, or so. In addition, many "rules of thumb" are based on specific designs, which may not apply to future or leveraged designs. Some rules of thumb were just plain lucky to have worked.

PC boards must be designed from a physics point of view and the most important consideration is that high frequency signals, clocks, and power distribution networks (PDNs) must be designed as transmission lines. This means that the signal or energy transferred is propagated as an electromagnetic wave. PDNs are a special case, as they must carry both DC current and be able to supply energy for switching transients with minimal simultaneous switching noise (SSN). The characteristic impedance of PDNs is designed with very low impedance (0.1 to 1.0 Ohms, typically). Signal traces, on the other hand, are usually designed with a characteristic impedance of 50 to 100 Ohms.

The previous article introduced the concept of the circuit theory and field theory viewpoints. A successful PC board design accounts for both viewpoints. Circuit theory suggests that current flows in loops from source to load and back to the source. In many cases of product failure, the return path has not been well defined and in some cases, the path is broken. Breaks or gaps in the return path are major causes of radiated emissions, radiated susceptibility, and ESD failures.

Correspondingly, electric fields on PC boards exist between two pieces of metal, such as a microstrip over a return plane (or trace). If the return path is broken, the electric field will "latch on" to the next closest metal and will not likely be the return path you want. When the return path is undefined, then the electromagnetic field will "leak" throughout the dielectric and cause common mode currents to flow all over the board, as well as cause cross-coupling of clocks or other high speed signals to dozens of other circuit traces within that same dielectric.

*Figure 1* shows a propagating wave within the dielectric between the signal trace and return plane (or trace). This shows both the conduction current flowing in the signal trace and back on the return plane (or trace) and the displacement current "through" the dielectric. The signal wave front travels at some fraction of the speed of light as determined by the dielectric constant. In air, signals travel at about 12 inches per nanosecond. In the typical FR4 dielectric, the speed is about half that at 6 inches

per nanosecond. Refer to *Reference 1, 2*, and *3* for more information on the physics of signal propagation through PC boards.

![](_page_12_Figure_10.jpeg)

Figure 1 - A propagating wave along a microstrip with reference plane. Figure, courtesy Eric Bogatin.

In order to satisfy both the circuit and field theory viewpoints, we now see the importance of adjacent power and power return planes, as well as adjacent signal and signal return planes. PDN design also requires both bulk and decoupling "energy storage" capacitors. The bulk capacitors 4.7 to 10 μF, typ.) are usually placed near the power input connector and the decoupling capacitors (1 to 10 nF, typ) nearest the noisiest switching devices - and most importantly, with minimal trace length connecting these from the power pins to signal return plane. Ideally, all decoupling capacitors should be mounted right over (or close to) the connecting vias and multiple vias should be used for each capacitor to reduce series inductance.

Signal or power routed referenced to a single plane will always have a defined return path back to the source. *Figure 2* shows how the electromagnetic field stays within the dielectric on both sides of the return plane. The dielectric is not shown for clarity.

![](_page_12_Figure_14.jpeg)

Figure 2 - A signal trace passing through a single reference plane.

On the other hand, referring to *Figure 3*, if a signal passes through two reference planes, things get a lot trickier. If the two planes are the same potential (for example, both are return planes), then simple connecting vias may be added adjacent to the signal via. These will form a nice defined return path back to the source.

If the two planes are differing potentials (for example, power and return), then stitching capacitors must be placed adjacent to the signal via. Lack of a defined return path will cause the electromagnetic wave to propagate throughout the dielectric, causing cross coupling to other

signal vias and leakage and radiation out the board edges as shown.

![](_page_13_Figure_2.jpeg)

Figure 3 - A signal trace passing through two reference planes. If the reference planes are the same potential (signal or power returns, for example), then stitching vias next to the signal via should be sufficient. However, if the planes are different potentials (power and return, for example), then stitching capacitors must be installed very close to the signal via. Lack of a defined return path will cause the electromagnetic field to leak around the dielectric, as shown, and couple into other signal vias or radiate out board edges.

For example, let's take a look at a poor (but very typical) board stack-up that I see often. See *Figure 4*.

![](_page_13_Figure_5.jpeg)

Figure 4 - A six-layer board stack-up with very poor EMI performance.

Notice the power and power return planes are three layers apart. Any PDN transients will tend to cross couple to the two signal layers in between. Similarly, only signal layers 1 and 3 have an adjacent return plane. Signal layers 4 and 6 are referenced to power, rather than signal return, therefore, the propagating wave return path will jump all over to whatever is the closest metal on the way back to the source, which is referenced to signal return. Again, this will tend to couple clock and other digital noise throughout the board.

![](_page_13_Figure_8.jpeg)

Figure 5 - A six-layer board stack-up with good EMI performance. Each signal layer has an adjacent return plane and the power and power return planes are adjacent.

A better design is shown in *Figure 5*. Here, we lose one

signal layer, but we see the power and power return planes are adjacent, while each signal layer has an adjacent signal (or power) return plane. It's also a good idea to run multiple connecting vias between the two return planes in order to guarantee the lowest impedance path back to the source. The EMI performance will be significantly improved using this, or similar designs. In many cases, simply rearranging the stack-up is enough to pass emissions.

Note that when running signals between the top and bottom layers, you'll still need to include "stitching" vias between the return planes and stitching capacitors between the power and power return planes right at the point of signal penetration in order to minimize the return path. Ideally, these stitching vias should be located within 1 to 2 mm of each signal via.

**Other Tips** - Other design tips include placement of all power and I/O connectors along one edge of the board. This tends to reduce the high frequency voltage drop between connectors, thus minimizing cable radiation. Also, segregation of digital, analog, and RF circuits is a good idea, because this minimizes cross coupling between noisy and sensitive circuitry in the return plane.

Of course, high-speed clocks, or similar high-speed signals, should be run in as short and as direct a path as possible. These fast signals should not be run long board edges or pass near I/O or power connectors.

**Gaps in Return Plane** - I'd like to come back to the gap or slot in the return plane mentioned earlier and show an example of why it's bad news for EMI. When the return path is interrupted, the conduction current is forced around the slot, or otherwise finds the nearest (lowest impedance) path back to the source. The electromagnetic field is forced out and the field will "leak" all over the board. I have an article and good demonstration video of this and how it affects common mode currents and ultimately, EMI. See *Figure 6* and *Reference 4*.

![](_page_13_Figure_16.jpeg)

Figure 6 - shows a demonstration test board with transmission lines terminated in 50 Ohms. One transmission line has a gap in the return plane and the other doesn't. A harmonic comb generator (2 ns pulse) is connected to one of the two BNC connectors in turn and the harmonic currents in a wire taped to the return plane are measured with a current probe.

The difference between the gapped and un-gapped traces is shown in *Figure 7*. Note the harmonic currents are 10 to 15 dB higher for the gapped trace (in red). Failing to pay attention to the signal and power return paths is a major cause of radiated emissions failures.

![](_page_14_Figure_2.jpeg)

Figure 7 - The resulting common mode currents on an attached wire (to the return plane) as measured with a current probe. The trace in aqua is the ungapped return path and the trace in red, the gapped return path. The difference is 10 to 15 dB higher for the gapped return path. These harmonic currents will tend to radiate and will likely cause radiated emissions failures.

#### **SHIELDING**

The two issues with shielded enclosures is getting all pieces well-bonded to each other and to allow power or I/O cable to penetrate it without causing leakage of common mode currents. Bonding between sheet metal may require EMI gaskets or other bonding techniques. Slots or apertures in shielded enclosures become issues when the longest dimension approaches a half wavelength.

![](_page_14_Figure_6.jpeg)

Figure 8 - A chart of attenuation versus slot length. Figure, courtesy Henry Ott.

*Figure 8* shows a handy chart for determining the 20 dB attenuation of a given slot length. For example, if a product design requires at least a 20 dB shielding effectiveness, then the longest slot length can be just one-half inch. See *Reference 5* and *6* for more detail on shielding. Interference Technology also has a free downloadable 2017 EMI Shielding Guide with excellent information (*Reference 7*).

*Figure 9* is a chart of wavelength versa half wave resonance at 1000 MHz. This is a handy tool for determining how efficient a cable or slot will act as an antenna.

![](_page_14_Figure_11.jpeg)

Figure 9 - A handy chart for determining resonant frequency versus cable or slot length in free space. Half-wavelength slots simulate dipole antennas and are particularly troublesome. Figure, courtesy Patrick André.

**Cable Penetration** - The number one issue I find when tracking down a radiated emissions problem is cable radiation. The reason cables radiate is that they penetrate a shielded enclosure without some sort of treatment - either bonding the cable shield to the metal enclosure or common mode filtering at the I/O or power connector (*Figure 10* and *11*). This occurs frequently, because most connectors today are attached directly to the circuit board and are then poked through holes in the shield. Once the cable is plugged in, it is "penetrating the shield" and EMI is the usual result.

![](_page_14_Figure_14.jpeg)

Figure 10 - Penetrating the shield with a cable defeats the shield. This example shows how external energy sources can induce noise currents in I/O cables, which can potentially disrupt internal circuitry. The reverse is also true, where internal noise currents can flow out the cable and cause emissions failures. Figure, courtesy Henry Ott.

There are four combinations or cases that must be considered: shielded or unshielded products, and shielded or unshielded cables. Power cables are usually unshielded for consumer/commercial products and so require power line filtering at the point of penetration or at the connector of the circuit board. Shielded cables must have the shield bonded (ideally in a 360 degree connection) to the product's shielded enclosure. If the product does not have a shielded enclosure, then filtering must be added at the point of penetration or at the I/O connector of the PC board. *Figure 11* shows the usual result when connectors simply poke through a shielded enclosure.

![](_page_15_Figure_2.jpeg)

Figure 11 - Result of a penetrating cable through a shielded enclosure, because of un-bonded I/O connectors to the shielded enclosure.

**Cable Shield Terminations** - Another potential issue is if the I/O cable uses a "pigtail" connection to the connector shell. Ideally, cable shields should be terminated in a 360-degree bond for lowest impedance. Pigtails degrade the cable shield effectiveness by introducing a relatively high impedance. For example, a 1-inch pigtail connection has 12 Ohms impedance at 100 MHz and gets worse the higher you go in frequency. This is especially problematic for HDMI cables, because the HDMI working group (http://www.hdmi.org) originally failed to specify the method for terminating the cable shield to the connector. This may have been corrected in the latest edition of the standard released in 2017.

## **FILTERING**

I won't go into very much detail here, because Interference Technology has an excellent EMI Filter Guide free for the downloading (see *Reference 8*). Suffice to say, filters, as well as transient protection, are important at power and I/O connectors. Typically, these will be common mode topologies, as shown in *Figure 12*. Most signal-level common mode chokes may be obtained in surface mount packaging. Power chokes are much larger to handle the current and may be obtained as either surface mount or through-hole mount, depending on the current rating. Many Ethernet connectors also have built-in common mode filtering.

Power supply input filters are generally designed to suppress both differential and common mode currents. A typical topology is shown in *Figure 13*. The "X" capacitor is designed to filter differential mode, while the CM choke and "Y" capacitors are designed to filter common mode. The resistor shown is usually 100 kOhm and the purpose is merely to bleed off the line voltage stored on the capacitors to a safe level.

![](_page_15_Figure_9.jpeg)

![](_page_15_Figure_10.jpeg)

![](_page_15_Figure_11.jpeg)

Figure 13 - A general purpose filter typically used for power supply input filtering.

![](_page_15_Figure_13.jpeg)

Figure 14 - Five common filter topologies, depending on the source and load impedances. Figure, courtesy Würth Electronik.

For general purpose filtering of signals, the handy chart of possible filter topologies may be found in Reference 9 and

is reproduced here in *Figure 14*. The appropriate topology depends on the source and load impedances. If these impedances are not known, then either the "PI" or "T" topology may be used (#3 or #5 on the chart, respectively).

Ferrite or inductive components should not be used in series with the power pins of ICs, as this will only reduce the ability of the local decoupling capacitors to supply required energy during simultaneous switching of the IC output stages with the resulting higher power supply noise. If used, they should be inserted "upstream" from the bulk capacitor.

**Ferrite Chokes** - One common filter element usually added to I/O cables is the ferrite choke. Ferrite chokes come in either the clamp-on types or solid cores meant to be assembled along with the cable assembly. Often, these are used as a last resort to reduce cable emissions or susceptibility.

Ferrite chokes have an associated impedance versus frequency characteristic, often peaking around 100 to 300 MHz. Some materials are designed to peak below 100 MHz for lower frequency applications. Maximum impedances can range from 25 to 1000 Ohms, depending on the ferrite material used and style of choke.

You may have noticed that clipping a ferrite choke onto a cable sometimes has no effect. This is usually due to the fact the choke has the same, or lower, effective impedance than the source and load impedances. The attenuation of a ferrite choke is easily calculated.

Attenuation (dB) = 20  $*$  log((Zin + Zferrite + Zload) / (Zin + Zload))

For example, if we add a 100 Ohm ferrite choke to a power supply cable with system impedance of 10 Ohms (source and load), the attenuation would be:

Attenuation =  $20 * log((10 + 100 + 10)/(10 + 10)) = 15.5 dB$ 

Refer to *Reference 9* for much additional detail on ferrite chokes and general filter design.

# **TRANSIENT PROTECTION**

In order to protect internal circuitry from electrical transients, such as ESD, electrically fast transient (EFT), or power line surge, due to lightning, transient protective devices should be installed at all power and I/O ports. These devices sense the transient and "clamp" the transient pulse to a specified clamp voltage.

Transient protectors in signal lines must generally have a very low parallel capacitance (0.2 to 1 pF, typical) to the return plane (or earth ground), depending on the data rate in order to maintain signal integrity. These silicon-based devices may be purchased in very small surface mount packaging.

Power line surge protection usually requires much larger transient protection devices and they can come in a variety of types. Gas discharge or metal oxide varistors are the most common, but larger silicon-based devices are also available. More information on the design of surge protection may be found in *Reference 9*.

# **SUMMARY**

Most EMC/EMI failures are due to poor shielding, penetration of cables through shields, poor cable shield termination, poor filtering, and above all, poor PC board layout and stack-up. Paying attention to these common design faults will pay off with a lower risk of compliance failures and result in lower project costs and schedule slippage.

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![](_page_16_Figure_26.jpeg)

![](_page_17_Picture_0.jpeg)

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# BASICS OF PASSIVE FILTERS FOR EMC COMPLIANCE

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# *Introduction*

One of the roles of the practicing EMC engineer or product designer is to be able to design filters to add to circuits in order to get them to pass various EMC immunity and emissions standards such as IEC 61000-4-2 for ESD immunity, IEC 61000-4-3 for Radiated RF immunity and IEC 61000-4-4 for Electrical Fast Transient/Burst immunity and other various international standards covering Radiated Emissions (RE) or Conducted Emissions (CE). EMI filters are often used along with proper shielding in order to achieve EMC compliance. The purpose of a filter is to establish either a low-impedance path for RF current to return back to the local source of energy, and/or to provide a high impedance to prevent RF currents from flowing on a cable. However, selecting the proper filter for a given situation may be confusing to some, especially if they are new to the EMC field or have not dealt with the subject in some time. EMC practitioners may be asking themselves what filter configuration is the best one to use for any given application or *how to correctly choose the values of components given the frequency, circuit impedance, and other parameters*  of the circuit. They may also want to know how they can get more attenuation out of their filter design in order to pass an emissions or immunity test. The time to learn how to properly design filters for EMC compliance is not when schedules are tight, and the product's ship date is rapidly approaching. If you find yourself stuck in any of the above situations, this article on passive filter basics for EMC compliance should help remove the mystery, and allow you to quickly find the best passive component filter solution that allows product to ship on time.

![](_page_18_Picture_5.jpeg)

# BASICS OF PASSIVE FILTERS FOR EMC COMPLIANCE

# **PASSIVE LOW-PASS FILTERS**

Fortunately, designing filters for EMC compliance is not as difficult as it may seem. For most cases, in order to achieve EMC compliance, we really only need to know how to apply passive low-pass filter types to our circuits. The other types of passive filters, such as high-pass, band-pass, and band-reject are not as common as the low-pass filter is for EMC work and will not be covered in this paper. Consult the references for more information on these other filter types.

Unfortunately, circuit impedances are not always well understood or impossible to know, making it more difficult to determine which values of passive low-pass filter components to choose from in order to pass the EMC compliance tests. This is the situation with common mode emissions emanating off of a cable during a RE test where the impedance of the cable changes as it is rearranged in order to maximize emissions (*Reference [1]*).

It is impossible to model the filter exactly if the load impedance is not known. The only way to know if a lowpass filter design is adequate or not is by trial and error experiments performed during EMC compliance testing, or more preferably, by trying out different low-pass filter component values very early in the product development cycle. In order to be most effective, this experimental work should occur during pre-compliance testing performed in your own test facility prior to going out of house for full-compliance testing. See *Reference [3]* for a detailed description on how to setup an in-house pre-compliance EMC test facility.

A low-pass filter is one in which the frequencies below a certain significant frequency are easily let-through and those above this same significant frequency are heavily attenuated. A passive low-pass filter is a simple voltage divider; non-amplifying device composed of a combination of resistors and capacitors, inductors (or ferrites) and capacitors or in some instances, may be composed of just one of these components. For instance, a single capacitor placed across a line to reference ground without the resistor or inductor installed may be all that is required in order to suppress an unwanted signal.

The benefit to using a single component filter is that only one physical device is required which in turn requires less board space and also helps keep parts costs down. Multi-element filters are useful in situations where the range of frequencies involved is too large and impossible for a one component filter to fully attenuate.

# **RC LOW-PASS FILTER**

One of the most basic forms of a low-pass filter is comprised of just one resistor and one capacitor, an RC filter. In an RC low-pass filter, the cutoff frequency occurs at resonance, where the capacitive reactance  $(X_c)$  equals the resistance (R) and where X<sub>c</sub> =1/2πfC (*Reference [4]*).

A simple RC low-pass filter and the equation for determining its cutoff frequency is shown in *Figure 1*. Note that the filter shown in *Figure 1* is also known as an L filter due to its resemblance to the letter L. It is also considered a single-pole filter because there is only one reactive component, the capacitor.

![](_page_19_Figure_12.jpeg)

Figure 1: Basic RC Low-Pass Filter (L Type)

A low-pass filter has an ideal, theoretical response where all signals contained below a so-called critical frequency (the 3 dB down point) are easily let-through the device and above which frequency, all signals are heavily attenuated. An ideal low-pass filter response curve is shown in *Figure 2*.

![](_page_19_Figure_15.jpeg)

Figure 2: Ideal low-pass filter response curve

In actual practice, the output of the filter will not go to zero as abruptly as shown in the ideal curve of *Figure 2*. In actuality, the output will gradually roll off at a 6 dB/octave or 20 dB/decade rate as shown in *Figure 3*.

# **EMC APPLICATION OF LOW-PASS FILTERS**

*Reference [3]* suggests applying a low-pass filter in order to fix an EMC problem such as a fast transient or ESD discharge immunity issue and that a good starting point in putting together a low-pass filter that will work for most situations is to start out by using a 47 to 100 $\Omega$  series resistor placed in the signal line, with a 1 to 10nF capacitor placed in the signal or power return line. If we take this in-

formation and select R = 100Ω and C = 10nF as a starting point, the cut-off frequency  $(f_{\infty})$  will equal approximately 159 kHz, and the low-pass filter response curve should look like that shown in *Figure 3.* Very little of the signals that are greater than 1.59 MHz will be let through the filter as they are 20 dB lower than any of the signals that at the filter's cutoff frequency of 159 kHz.

As another example, if we leave  $R = 100\Omega$  and select C = 1nF, the cutoff frequency at the 3 dB down point moves out to roughly 1.59 MHz, the 6 dB down point is at 3.2 MHz, and the signal is almost completely attenuated at 15.9 MHz. Signals greater than 15.9 MHz are heavily attenuated and not let through the filter.

*Table 1* contains a matrix of the various R-C low-pass filter values discussed so far plus some others that might be useful, and their low-pass filter characteristic responses at the 6 dB and 20 dB down points.

When attempting to suppress an unwanted high-frequency signal, one may find out that a filter containing only a single reactive component (i.e. one capacitor or one inductor) may not provide enough attenuation. Adding a second reactive component will increase the roll off to 12 dB/octave or 40 dB/decade (*Reference [4]*). These types of filters are called various names such as double-pole, two-stage, two-element, or second-order filters. Filters with three reactive components will provide 18 dB/octave or 60 dB/decade attenuation. Four reactive component filters will provide 24 dB/octave or 80 dB/decade attenuation and so on (*Reference [2]*).

![](_page_20_Figure_5.jpeg)

Figure 3: Realistic low-pass filter response curve

![](_page_20_Picture_314.jpeg)

Table 1: Matrix of R-C Values and Low-Pass Filter Reponses

# **SELECTION OF F<sub>co</sub>**

When selecting a cut-off frequency for a low-pass filter, it is important to take into account the fundamental frequency of the intended data, clocks, and other purposeful signals present on the filtered line. If the cut-off frequency chosen is too low in frequency, then the intended signals will be attenuated along with the higher frequency signals that you want to suppress. Try to maintain at least the 5<sup>th</sup> harmonic of the intended signal, with the 10th harmonic being ideal (*Reference [3]*). Many I/O signals that are used with unshielded cables require some form of filtering in order to be in compliance with EMC standards. These signals usually have a frequency of 1 MHz or less (*Reference [1]*). It is important to also ensure that by adding a filter's impedance to circuit that it does not in turn create a signal integrity problem.

Once the filter's component values are chosen, carefully consider where it is going to be placed in the circuit or system. The most benefit is obtained when the filter is placed as close to the item to be protected as possible, one centimeter is ideal for most designs (*Reference [1]*). In order to keep any extra unwanted inductance from affecting performance of the filter, be sure to keep lead lengths as short as possible. Additional layout and placement concerns will be covered later in this article.

# **USE OF FERRITES**

If the voltage drop across the series resistor cannot be tolerated, a device such as a ferrite, which acts as a high-frequency resistor with minimal voltage drop, can be used instead of the resistor. Because the ferrite presents the circuit with high AC impedance, while also not affecting signal quality, they are most optimal for filtering at frequencies greater than 30 MHz. Carefully consider the amount of DC or low-frequency current present in the circuit when using ferrites. They can become easily saturated with too much current present in the circuit which renders them ineffective (*Reference [5]*).

# **USE OF INDUCTORS**

An inductor can also be considered for the series element in a low-pass filter instead of a resistor or ferrite, particularly if dealing with a signal in the 10 to 30 MHz range. When using inductors, beware of the effect that their inductive reactance (XL = 2πfL) and parasitic capacitance will have at these higher frequencies. You may be actually creating a high-pass filter when you are attempting to create a low-pass one, and not even realize it.

# **BASIC FILTER TOPOLOGIES**

The following diagrams show two more of the basic filter configurations available for impedance mismatching between circuit source and load input and output impedances and filter input and output impedances. Both are named after their shapes. The first is called a  $π$  filter because it looks like the Greek letter π and the second is called the T filter because it looks like the letter T. Note

that there are three reactive elements present in these filters which means they an attenuation curve of 18 dB/ octave and 60 dB/decade. They are considered third-order filters (*Reference [5]*).

![](_page_21_Figure_2.jpeg)

#### **IMPEDANCE MISMATCHING**

Source and load impedances must be considered in selecting the proper filter configuration. If order to work properly, the source driving the input to the low-impedance shunt element (i.e. capacitor), should be a high-impedance. If the output of the source is a low-impedance, it should face the high-impedance series component. This same concept applies to load input impedances versus the filter's output impedances. In general, a source or load impedance less than 100  $\Omega$  is considered low and great than 100Ω is considered high impedance (*Reference [5]*). *Table 1* provides a matrix of source versus load impedances and their associated correct filter topologies.

![](_page_21_Picture_366.jpeg)

# **DIFFERENTIAL MODE (DM) AND COMMON MODE (CM) CURRENTS**

There are two different types of current modes, and hence noise sources capable of creating interference. It is important to know which mode is prevalent so that

proper filtering can be applied. The two types of signals we are referring to are differential mode (DM) and common-mode (CM) signals.

DM signals carry useful information whereas CM currents provide no useful information what-so-ever and are the main source of RE and CE issues. A DM signal travels down one side of a circuit path, and an equal and opposite DM signal travels back on the other side of the path. If no circuit discontinues exists, then complete canceling of these two DM signals occur, and no CM current is developed. Placing capacitors across the outgoing and return lines and/or an inductor in series with either outgoing or return line is called DM filtering.

CM signals are in-phase signals present in both outgoing and return lines of a circuit. They do not cancel each other out but add up, often to a level substantial enough to cause EMI issues. CM filtering involves placing capacitors across each signal line to ground reference and sometimes also using a CM inductor in the circuit. The CM inductor only acts on the CM signals that are present. It does not affect the DM signals.

# **PARASITICS**

The non-ideal behavior of the elements that make up our filter must be addressed. Unexpectedly, we will find that real capacitors and inductors possess both capacitance and inductance which limits the bandwidth that they are useful over. The amount of parasitics present in a circuit can be reduced through proper component selection and layout techniques, but cannot be eliminated entirely. As frequency increases, the reactance of a capacitor decreases until it reaches its self-resonant frequency. Up to this point, the capacitor is behaving as it should – it behaves like a resistor. Above its self-resonant frequency point the capacitor becomes inductive and it acts like an inductor because of the parasitic inductance found in its metal plates. This parasitic effect is greater in leaded types of capacitors than it is with the surface mount technology (SMT) types that have almost no lead length.

The opposite effect occurs with an inductor where its reactance becomes capacitive above its self-resonant frequency point, and where the inductor now acts like a capacitor. At the self-resonant frequency, capacitors are intended to provide a very low impedance and inductors should provide a high impedance. For inductors, their limiting factors are related to the parasitic capacitance present between each winding and overall capacitance located between one lead and the other.

The inductor's inter-winding parasitic capacitance is not as big a deal in regards to effectiveness for EMI suppression as is a capacitor's parasitic inductance. The main factors that change the intended behavior of capacitors is the parasitic inductance of the circuits in which they are installed, not necessarily the construction of the ca-

pacitor. Therefore, proper layout and placement then becomes the critical factor when attempting to effective utilize passive low-pass filters for EMI suppression.

![](_page_22_Figure_2.jpeg)

# **LAYOUT AND PLACEMENT CONCERNS**

Because there is going to be unknown and hidden parasitics involved, do not expect your filter design to work one-hundred percent the first time. As mentioned earlier, expect the need to perform some trial and error design and troubleshooting in the lab. If not available already, have on hand a selection of various components that you want to try out. Do not wait until the last minute to obtain the SMT capacitors, inductors, or ferrites that you want to use. Make sure the components selected are designed for the bandwidths involved. Create your own matrix of values, critical frequencies, and 6- and 20-dB roll-off curves.

In reviewing the layout, look for longer than necessary trace lengths that add extra inductance and impedance. When applying fixes, be sure keep connections short. If an R-C filter is added to the reset pin of a micro-controller, place it as close to the pin as possible and do not overlook the length of its return trace. In general, it is best to locate the filter as close to the offending signal source as possible, not some obscure location far away.

Watch out for trace or wire routing that allows for too much capacitive and inductive coupling to other noisy signal or traces. Filter components should be placed right at an entry connector (I/O and power inputs). Placement of a filter deeper inside a circuit or system allows EMI to enter the system (*Reference [6]*). If separation is not maintained, improper routing of input and output sections can mean that filter elements are essentially bypassed and no longer effective. On PCBs, capacitors should shunt unwanted signals to chassis not line to line or line to return (*Reference [6]*). It is best to understand the path of current flow and to not necessarily rely on "ground" as being the ultimate zero-ohm impedance and sole problem savior.

Finally, although they appear to be useful and easy to troubleshoot with, do not expect too much out of clampon ferrite common-mode chokes as they only provide about 10 dB of attenuation (*Reference [3]*).

# **CONCLUSION**

The need to utilize passive low-pass filters to obtain EMC compliance is a given. They provide a low-impedance path for RF currents to return back to the local source of energy or provide a high impedance to prevent unwanted RF currents from flowing. A filter that does both is ideal. Designing low-pass filters for EMI suppression is not that difficult. Proper knowledge and planning before the need for them arises can save developers some time and headaches.

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# TOP THREE EMI AND POWER INTEGRITY PROBLEMS WITH ON-BOARD DC-DC CONVERTERS AND LDO REGULATORS

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Modern devices are continuing a long-term trend of squeezing more electronics into smaller packages, while also increasing system performance, data rates and operating efficiency. Higher efficiencies are often achieved by implementing faster silicon MOSFETs or even faster eGaN FETs while size is reduced by increasing switching frequencies and replacing aluminum and tantalum capacitors with smaller ceramic devices. One result of this trend is that there is greater interaction between the disciplines of EMI, signal integrity (SI) and power integrity (PI).

![](_page_24_Picture_5.jpeg)

# TOP THREE EMI AND POWER INTEGRITY PROBLEMS WITH ON-BOARD DC-DC CONVERTERS AND LDO REGULATORS

# **INTRODUCTION**

EMI is a measure of the electromagnetic emissions produced by the high-speed current and voltage signals the system creates. Power integrity is a measure of the power quality at the device that being powered. This means that the power supply voltages must be maintained within the allowable operating voltage range of high-speed devices. Devices, such as modems, reference clocks and low noise amplifiers (LNAs) are all sensitive to noise on the power rails, which results in timing jitter, spurious responses reduced data channel eye openings, and degraded signal-to-noise ratio (SNR). This too, is a measure of power integrity. The power supply itself is a noise source and the noise sources generated by the power supply must be kept from propagating through the system.

This article discusses the three most common causes of EMI and power integrity issues while providing tips for how to avoid or minimizes them in your design,

- **1. Ringing** on switched waveforms causes broad resonant peaks in the emission spectrum.
- **2. DC-DC converters generate noise** at the switching frequency, and because of high speed switching devices, can generate broadband switching harmonics well into the GHz.
- **3. Power plane resonance** in DC-DC converter or LDO regulators due to high-Q capacitors resonating with power planes.

# **RINGING AND RADIATED EMISSIONS**

Any ringing on the switched waveform (fairly common) can lead to broadband resonances in the resulting RF spectrum. Resonant frequencies resulting from DC-DC converters or low dropout (LDO) linear regulators can be as low as a few kHz while resonance due to the PDN with switching devices, such as MOSFET's can be in hundreds of MHz or higher.

The harmonic energy resulting from this switching is "captured" by the PDN and device resonances, evident as ringing in the time domain. The current and voltage of this ringing produces EMI. The magnitudes of the ringing and EMI are related to the quality factor (Q) and characteristic impedance of the resonance and the harmonic energy produced by the switching.

As an example, the switching waveform on a DC-DC buck converter demo board was measured with a Rohde & Schwarz RTE 1104 oscilloscope and Rohde & Schwarz RT-ZS20 1.5 GHz active probe (*Figure 1*).

![](_page_25_Figure_12.jpeg)

Figure 1. Diagram showing the measuring point at the switch device junction (on the left side of L1) to ground return.

There was a very large ringing superimposed on the switched waveform of 216 MHz. This can be seen clearly in *Figure 2*.

A Fischer Custom Communications F-33-1 current probe was used to measure both the input power cable common mode current (violet trace) and output load differential mode current (aqua trace). See *Figure 3*. Note the broad resonant peaks at 216 MHz (marker 1) and the second harmonic at 438 MHz (marker 2).

![](_page_25_Picture_16.jpeg)

Figure 2. Measuring the rise time and ringing on a DC-DC converter. Notice to strong ringing at 216 MHz.

![](_page_25_Figure_18.jpeg)

Figure 3. Resulting resonances from the 216 MHz ring frequency (marker 1) and second harmonic at 438 MHz (marker 2).

**Remediation Tips** - There are several ways to improve the design to minimize the resonances, ringing and therefore EMI. Since the energy is related to the switching frequency, rise time of the switching, characteristic impedance, and Q of the resonances, these factors are also the paths to mitigation.

- Slower edges will degrade operating efficiency but reduce high frequency energy
- Careful PCB design and capacitor selection will minimize the characteristic impedance and Q
- Keep traces short and wide and dielectrics thin.
- Keep all the switching circuitry on one side of the board, preferably with a thin dielectric to the respective ground return plane.
- Use of a snubber circuit, damping of resonances using controlled ESR capacitors, or redesign of the inductor for lower leakage inductance.

For additional detail on measuring ringing refer to *Reference 1*.

# **FAST EDGES CREATE BROADBAND NOISE AT GHZ FREQUENCIES**

Today's on-board DC-DC converters use switching frequencies as high as 3 MHz. This is an advantage because it allows for physically smaller inductor and filter components, as well as increased efficiency. However, the fast edge speeds create broadband harmonic energy. The bandwidth of this harmonic energy is related to the voltage and current rise time. A 1ns edge speed can produce harmonic energy up to 3 GHz, or more.

These broadband harmonics are the cause of radiated emissions failures and also can affect the receiver sensitivity of any on-board telephone modems or other wireless systems, such as GPS. *Figure 4* shows how a typical DC-DC converter circuit can be characterized using an H-field probe connected to a spectrum analyzer.

It's also possible to connect the probe to an oscilloscope and hold it near each DC-DC converter to get some idea of the ringing, if any, without disturbing the circuit.

![](_page_26_Picture_12.jpeg)

Figure 4. Probing DC-DC converter noise sources on a typical wireless device.

*Figure 5* shows the resulting measurement of a couple DC-DC converters. The yellow trace is the ambient noise floor of the measurement system and is always a good idea to record for reference. The aqua and violet traces are the two converter measurements. Note that both produce broadband noise currents out to 1 GHz, with the convertor in violet out to beyond 1.5 GHz. Note the violet trace is 20 to 50 dB higher than the ambient noise floor.

![](_page_26_Figure_15.jpeg)

![](_page_26_Figure_16.jpeg)

**Remediation Tips** – To reduce the risk of self-interference to on-board mobile phone modems and wireless systems, the product design must start off with EMC in mind and with no corners cut. This will consist of:

- A near perfect PC board layout
- Filtering of DC-DC converters
- Filtering of any high frequency device
- Filtering of the radio module
- Local shielding around high noise areas
- Possibly shielding the entire product
- Proper antenna placement

The PC board layout is critical and is where most of your effort should reside. An eight or ten layer stack-up will provide the most flexibility in segregating the power supply, analog, digital, and radio sections and provide multiple ground return planes, which may be stitched together around the board edge to form a Faraday cage. Care must be taken to avoid return current contamination between sections – especially in the ground return planes. For wireless products, the power plane for the radio modem section should be isolated (except via a narrow bridge) from the digital power plane. All traces to this isolated plane should pass over the bridge connecting the two. This can provide up to 40 dB of isolation between the digital circuitry and radio.

It is vital that the power and ground return planes be on adjacent layers and ideally 3-4 mils apart at the most.

This will provide the best high frequency bypassing. All signal layers should be adjacent to at least one solid ground return plane. Clock, or other high-speed traces, should avoid passing through vias and should not change reference planes.

Power supply sections should be well isolated from sensitive analog or radio circuitry (including antennas). Be aware of primary and secondary current loops and their return currents. These return currents should not share the same return plane paths as digital, analog, or radio circuits. Remember that high frequency return currents want to return to the source directly under the source trace.

For more details on resolving DC-DC converter noise issues with wireless radio modems, refer to *Reference 2*.

# **PC BOARD PLANE RESONANCE AND THE EFFECT ON RADIATED EMISSIONS**

Noise propagation in a simple system can be represented by three elements, the voltage regulator, the printed circuit board planes with decoupling capacitors (PDN) and the device being powered (load).

Each of these three elements is comprised of resistive, inductive and capacitive terms. Even "noise free" low dropout (LDO) regulators can be highly inductive (*Reference 3*). The resistive, inductive and capacitive terms can resonate amplifying the noise signals created by the power supply and the load as they travel across the PDN creating EMI. The harmonics of the switching frequency and the switch ringing discussed earlier excite these PDN resonances (*Reference 4*). As stated previously this noise can degrade and interfere with on-board wireless modems, as well as resulting radiated and conducted emissions.

A short video helps explain the basic principles of PDN design (*Reference 5*). The radiated EMI of a LTC3880 DC-DC converter measured near the input plane using an H-field probe is seen in *Figure 6*.

![](_page_27_Figure_8.jpeg)

Figure 6. Spectrum analyzer display showing the 30 MHz and 160 MHz resonances detected near the input power connections of a DC-DC converter.

The 163 MHz is attributed to the ringing of the switches

as seen in *Figure 7*. This ringing is caused by the inductance of the upper MOSFET bond wires, pins and circuit board planes, ringing with the lower MOSFET and PC board capacitance.

![](_page_27_Figure_12.jpeg)

Figure 7. The 163 MHz EMI is easily explained by the ringing at the switch device, as discussed earlier.

The input ceramic decoupling capacitor resonates at approximately 30 MHz, as seen in *Figure 8* and results in the large 30 MHz EMI signature.

![](_page_27_Figure_15.jpeg)

![](_page_27_Figure_16.jpeg)

![](_page_27_Picture_17.jpeg)

Figure 9. The power plane section of the DC-DC converter (measured in Figure 6) with schematic representations of the component, PC board and external connections.

The input power plane section of the DC-DC converter (measured in *Figure 6*) is shown in *Figure 9* with schematic representations of the component, PC board and external connections.

A very simple simulation example can be used to illustrate these impedance resonance effects. Consider a simple DC-DC converter as shown in *Figure 10*.

![](_page_28_Figure_3.jpeg)

Figure 10. A simple DC-DC converter for illustration of plane resonance EMI. The "FET" switches include lead inductance and drain capacitance (Coss). A small PC board and two ceramic capacitors are included.

![](_page_28_Figure_5.jpeg)

Figure 11. The large round pins on the left are the input power connector, J2. The larger capacitor on the top side is an 0805 sized 47 μF and the smaller capacitor on the bottom side is an 0603 sized 0.1 μF.

Designers frequently place the FET switches on one side of the board with power entry on the opposite side of the PC board. The small PC board plane used in this example has power entry through a pair of pins and no interconnect inductance is added to connect power to the PC board. A large 47 μF ceramic capacitor is placed on the top side of the PC board, while a smaller, 0.1 μF ceramic capacitor is placed very close to the FET switches on the bottom side of the PC board. Two parallel vias connect power and ground from the top side of the PC board to the bottom side as seen in *Figure 11*.

The simple model is used to simulate the harmonic current in the input connector, which is directly related to conducted and radiated emissions. Two simulations are

performed; one with low ESR ceramic capacitors and the other with a lower Q controlled ESR ceramic replacing the 0.1 μF capacitor close to the FET switches. Both simulations are shown together in *Figure 12*.

![](_page_28_Figure_10.jpeg)

Figure 12. Spectral simulation of the input power lead shows the high Q ceramic (10 mΩ blue) has a clear peak near 10 MHz that is eliminated using a controlled ESR ceramic (200 mΩ red)

The simulated impedance, measured at the smaller capacitor in *Figure 13* shows the corresponding plane resonance with a clear 10 MHz peak using the high Q ceramic capacitor (blue) and the peak is eliminated using the controller ESR ceramic capacitor (red).

![](_page_28_Figure_13.jpeg)

Figure 13. The simulated impedance at the 0.1 uF capacitor using high Q ceramic (10 mΩ blue) and a controlled ESR ceramic (200 mΩ red)

**Remediation Tips** – To minimize PDN resonances, the complete system of voltage regulator, PDN and the load need to be carefully balanced. Damping resistance must be included to eliminate or minimize the existence or Q of resonances. This will consist of:

- Short, wide power planes
- Keep the layout as small as possible to minimize inductance
- Thinner PC board dielectric layers, closer to the surface
- Incorporate EM simulation to identify and minimize PDN resonances
- Keep capacitors on one side of the PC board to the extent possible
- Low-Q or ESR controlled capacitors reduce Q
- Choose voltage regulators and output capacitors for good control loop stability
- Don't place cutouts or holes in ground plane layers below the power plane
- Ferrite beads are a very common cause of PDN resonances
- Be aware of inductive interconnects bringing power to the system.

Printed circuit board design and decoupling is critical and "rules-of-thumb" generally don't work well in high speed circuits. The design of the circuit board and capacitor decoupling always involves trade-offs, but the impacts on resonances need to be weighed carefully. A multi-frequency harmonic comb generator can be extremely helpful for quickly identifying PDN resonances (*Reference 3*).

# **SUMMARY**

As you can see, designing DC-DC converters, LDOs, and PDNs with today's high-speed technology nearly always requires careful circuit design, adequate filtering, simulation of the PDN, very careful circuit board layout, and use of controlled-ESR filter capacitors. Poor designs can result in:

• Ringing in power supply switches (or other fastedged digital switching) resulting in associated radiated or conducted emissions resonant peaks at the ring frequency and harmonics.

- High frequency broadband noise well beyond 1 GHz, resulting in self-interference to radio modems.
- Poor stability and resonances in un-damped power distribution networks, leading to instability, spectral resonances, and associated radiated and conducted emissions.

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- 5. Sandler, How to Design for Power Integrity: Finding Power Delivery Noise Problems (Video), [https://www.youtube.com/watch?v=oL6qjhJH\\_](https://www.youtube.com/watch?v=oL6qjhJH_m4&t=4s&list=PLtq84kH8xZ9HIYgBYDsP7TbqBpftidzI8&index=4) [m4&t=4s&list=PLtq84kH8xZ9HIYgBYDsP7TbqBp](https://www.youtube.com/watch?v=oL6qjhJH_m4&t=4s&list=PLtq84kH8xZ9HIYgBYDsP7TbqBpftidzI8&index=4)[ftidzI8&index=4](https://www.youtube.com/watch?v=oL6qjhJH_m4&t=4s&list=PLtq84kH8xZ9HIYgBYDsP7TbqBpftidzI8&index=4)

![](_page_29_Picture_21.jpeg)

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![](_page_30_Picture_13.jpeg)

![](_page_30_Picture_14.jpeg)

# COMMON COMMERCIAL, AUTOMOTIVE, MEDICAL, WIRELESS & MILITARY EMC STANDARDS

# **►**COMMERCIAL STANDARDS

The following are some of the most common commercial EMC standards. Most standards have a fee associated and *most on the list are linked back to the source where they're available. If you're purchasing the printed version of* this guide, then refer to the Standards Organizations in the References section for standards purchase information. Note that many Euro Norm (EN) versions of IEC standards may be purchased at a considerable discount from the Estonian Centre for Standardization,<https://www.evs.ee>*.* 

# **FCC**

(<https://www.ecfr.gov>)

[Electronic Code of Federal Regulations \(e-CFR\)](https://www.ecfr.gov/cgi-bin/text-idx?SID=2fbdbc274cbc295d3b0e3106cace01c2&mc=true&tpl=/ecfrbrowse/Title47/47cfr15_main_02.tpl) [CFR 47 - Part 15 \(Radio Frequency Devices\)](https://www.ecfr.gov/cgi-bin/text-idx?SID=2fbdbc274cbc295d3b0e3106cace01c2&mc=true&tpl=/ecfrbrowse/Title47/47cfr15_main_02.tpl)

# ANSI

([http://webstore.ansi.org\)](http://webstore.ansi.org)

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# IEC

(<https://webstore.iec.ch>)

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[www.interferencetechnology.com](http://www.interferencetechnology.com) | 32 | Interference Technology Guide

![](_page_32_Picture_242.jpeg)

![](_page_33_Picture_206.jpeg)

# CISPR

(<https://webstore.iec.ch>)

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# **►**AUTOMOTIVE ELECTROMAGNETIC COMPATIBILITY STANDARDS

The following abbreviated list of automotive EMC standards was developed by Dr. Todd Hubing, Professor Emeritus of Clemson University Vehicular Electronics Lab ([http://www.cvel.clemson.edu/auto/auto\\_emc\\_standards.html](http://www.cvel.clemson.edu/auto/auto_emc_standards.html)*). A few of these standards have been made public and are linked below, but many others are considered company*  confidential and are only available to approved automotive vendors or test equipment manufacturers. While several *standards are linked on this list, an internet search may help locate additional documents that have been made*  public. For a more complete list, refer to the link above. Permission to republish has been granted.

# CISPR (AUTOMOTIVE EMISSIONS REQUIREMENTS)

([https://webstore.iec.ch\)](https://webstore.iec.ch)

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# ISO (AUTOMOTIVE IMMUNITY REQUIREMENTS)

(<https://www.iso.org>)

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![](_page_36_Picture_179.jpeg)

# SAE (AUTOMOTIVE EMISSIONS AND IMMUNITY)

(<http://standards.sae.org>)

![](_page_36_Picture_180.jpeg)

![](_page_37_Picture_170.jpeg)

# GM

[\(https://global.ihs.com\)](https://global.ihs.com)

![](_page_37_Picture_171.jpeg)

# FORD

[\(https://www.fordemc.com](https://www.fordemc.com))

![](_page_37_Picture_172.jpeg)

# DaimlerChrysler

![](_page_37_Picture_173.jpeg)

# Automotive Electromagnetic Compatibility Standards From

[<http://www.cvel.clemson.edu/auto/auto\\_emc\\_standards.html](http://www.cvel.clemson.edu/auto/auto_emc_standards.html)>

# **►**MEDICAL STANDARDS

# COLLATERAL STANDARDS

([https://www.webstore.iec.ch\)](https://www.webstore.iec.ch)

![](_page_38_Picture_141.jpeg)

# OTHER RELEVANT STANDARDS

(<https://www.webstore.iec.ch>)

![](_page_38_Picture_142.jpeg)

# For more extensive listings of medical standards, download the 2017 Medical EMC Guide:

<http://learn.interferencetechnology.com/2017-medical-emc-guide/>

# **►**COMMON WIRELESS STANDARDS

# ETSI STANDARDS

(<https://www.etsi.org>)

![](_page_39_Picture_190.jpeg)

# **►**COMMON MILITARY RELATED DOCUMENTS AND STANDARDS

*The following references are not intended to be all inclusive, but rather a representation of available sources of additional information and point of contacts. Downloadable from:* <http://everyspec.com>*.*

![](_page_39_Picture_191.jpeg)

[www.interferencetechnology.com](http://www.interferencetechnology.com) | 40 | Interference Technology Guide

![](_page_40_Picture_169.jpeg)

# **►**AEROSPACE STANDARDS

# AIAA STANDARDS

<http://www.aiaa.org/default.aspx>

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# RTCA STANDARDS

<https://www.rtca.org/>

![](_page_40_Picture_171.jpeg)

# SAE STANDARDS

[www.sae.org/](http://www.sae.org/)

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# [emc.live](http://www.emc.live)

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# REFERENCES

(ARTICLE LINKS, STANDARDS, BOOKS, MINI GUIDES, WEBSITES, & LINKEDIN GROUPS)

# **►**LINKS TO LONGER ARTICLES

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Lee, Basics on Designing for EMC Compliance, 2012 [https://interferencetechnology.com/basics-on-designing](https://interferencetechnology.com/basics-on-designing-for-emc-compliance/)[for-emc-compliance/](https://interferencetechnology.com/basics-on-designing-for-emc-compliance/)

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# McCune, CMOS Is Different: PCB Design for Both Low Noise and Low EMI, 2013

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# Armstrong, Cost-Effective EMC Design by Working With the Laws of Physics (Webinar), 2013

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# **►**EMC STANDARDS ORGANIZATIONS

**American National Standards Institute**  <http://www.ansi.org>

**ANSI Accredited C63**

<http://www.c63.org>

**Asia Pacific Laboratory Accreditation Cooperation (APLAC)**  <http://www.aplac.org>

# **BSMI (Taiwan)**

<https://www.bsmi.gov.tw/wSite/xslgip/chinese/index.html>

# **CISPR**

[http://www.iec.ch/emc/iec\\_emc/iec\\_emc\\_players\\_cispr.htm](http://www.iec.ch/emc/iec_emc/iec_emc_players_cispr.htm)

# **CNCA (China)**

[http://www.cnca.gov.cn/cnca/cncatest/20040420/](http://www.cnca.gov.cn/cnca/cncatest/20040420/column/227.htm) [column/227.htm](http://www.cnca.gov.cn/cnca/cncatest/20040420/column/227.htm)

## **Electromagnetic Compatibility Industry Association (UK)** <http://www.emcia.org>

**FDA Center for Devices & Radiological Health (CDRH)**  <https://www.fda.gov/MedicalDevices/default.htm>

**Federal Communications Commission (FCC)**  <http://www.fcc.gov>

**Gosstandart (Russia)** <http://gosstandart.gov.by/en-US/index.php>

# **IEC**

<http://www.iec.ch/index.htm>

# **IEEE Standards Association**

<http://www.standards.ieee.org>

# **IEEE EMC Society Standards Development Committee (SDCOM)**

[http://standards.ieee.org/develop/project/electromagnetic\\_](http://standards.ieee.org/develop/project/electromagnetic_compatibility.html) compatibility.html

**Industry Canada (Certifications and Standards)** [http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/h\\_sf06165.html](http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/h_sf06165.html)

# **ISO (International Organization for Standards)** <http://www.iso.org/iso/home.html>

**RTCA**

<https://www.rtca.org>

**SAE EMC Standards Committee** <http://www.sae.org>

**VCCI (Japan, Voluntary Control Council for Interference)** [http://www.vcci.jp/vcci\\_e/](http://www.vcci.jp/vcci_e/)

# **►**RECOMMENDED BOOKS

# ANDRÉ AND WYATT

#### **EMI Troubleshooting Cookbook for Product Designers**

SciTech Publishing, 2014. Includes chapters on product design and EMC theory & measurement. A major part of the content includes how to troubleshoot and mitigate all common EMC test failures.

# **ARCHAMBEAULT**

**PCB Design for Real-World EMI Control** Kluwer Academic Publishers, 2002.

# BOGATIN

## **Signal & Power Integrity - Simplified**

Prentice-Hall, 2018 (3rd Edition). Great coverage of signal and power integrity from a fields viewpoint.

# HALL, HALL, AND MCCALL

**High-Speed Digital System Design - A Handbook of Interconnect Theory and Design Practices** Wiley, 2000.

# JOFFE AND LOCK

## **Grounds For Grounding**

Wiley, 2010. This huge book includes way more topics on product design than the title suggests. Covers all aspects of grounding and shielding for products, systems, and facilities.

## JOHNSON AND GRAHAM

**High-Speed Digital Design -** 

**A Handbook of Black Magic**

Prentice-Hall, 1993. Practical coverage of high speed digital signals and measurement.

# JOHNSON AND GRAHAM

# **High-Speed Signal Propagation -**

**Advanced Black Magic**

Prentice-Hall, 2003. Practical coverage of high speed digital signals and measurement.

## KIMMEL AND GERKE

**Electromagnetic Compatibility in Medical Equipment** IEEE Press, 1995. Good general product design information.

## MARDIGUIAN

## **Controlling Radiated Emissions by Design**

Springer, 2016. Good content on product design for compliance.

## MARDIGUIAN

## **EMI Troubleshooting Techniques**

McGraw-Hill, 2000. Good coverage of EMI troubleshooting.

# MORRISON

# **Digital Circuit Boards - Mach 1 GHz**

Wiley, 2012. Important concepts of designing high frequency circuit boards from a fields viewpoint.

## MORRISON

**Grounding And Shielding - Circuits and Interference** Wiley, 2016 (6th Edition). The classic text on grounding and shielding with up to date content on how RF energy flows through circuit boards.

# **MORRISON**

## **Fast Circuit Boards - Energy Management**

Wiley, 2018. A brand new book explaining how electromagnetic energy moves through circuit boards. Destined to be a classic.

# OTT

# **Electromagnetic Compatibility Engineering**

Wiley, 2009. The "bible" on EMC measurement, theory, and product design.

# PAUL

**Introduction to Electromagnetic Compatibility** Wiley, 2006 (2nd Edition). The one source to go to for an upper-level course on EMC theory.

## SANDLER

#### **Power Integrity - Measuring, Optimizing, and Troubleshooting Power Related Parameters in Electronics Systems**

McGraw-Hill, 2014. The latest information on measurement and design of power distribution networks and how the network affects stability and EMC.

# SMITH AND BOGATIN

#### **Principles of Power Integrity for PDN Design - Simplified**

Prentice-Hall, 2017. Getting the power distribution network (PDN) design right is the key to reducing EMI.

## WILLIAMS

## **EMC For Product Designers**

Newnes, 2017. Completely updated text on product design for EMC compliance.

## **WESTON**

# **Electromagnetic Compatibility - Methods, Analysis, Circuits, and Measurement**

CRC Press, 2017 (3rd Edition). A comprehensive text, primarily focused on military EMC.

# WYATT & JOST

**Electromagnetic Compatibility (EMC) Pocket Guide** SciTech Publishing, 2013. A handy pocket-sized reference guide to EMC.

# **►**RECOMMENDED MINI-GUIDES FROM INTERFERENCE TECHNOLOGY (FREE DOWNLOADS)

# **NEW 2018 Components and Materials Guide**

[https://learn.interferencetechnology.com/2018](https://learn.interferencetechnology.com/2018-components-and-materials-guide/) [components-and-materials-guide/](https://learn.interferencetechnology.com/2018-components-and-materials-guide/)

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# **2017 EMC Filters Guide**

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# **2017 Medical EMC Guide**

[http://learn.interferencetechnology.com/2017-medical](http://learn.interferencetechnology.com/2017-medical-emc-guide/)[emc-guide/](http://learn.interferencetechnology.com/2017-medical-emc-guide/)

# **2017 Military and Aerospace EMC Guide**

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# **2017 Wireless Interference & RFI Guide**

[http://learn.interferencetechnology.com/2017-wireless](http://learn.interferencetechnology.com/2017-wireless-interference-rfi-guide/)[interference-rfi-guide/](http://learn.interferencetechnology.com/2017-wireless-interference-rfi-guide/)

# **2016 Real-Time Spectrum Analyzers Guide**

[http://learn.interferencetechnology.com/2016-real-time](http://learn.interferencetechnology.com/2016-real-time-spectrum-analyzer-guide/)[spectrum-analyzer-guide/](http://learn.interferencetechnology.com/2016-real-time-spectrum-analyzer-guide/)

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# **►**RECOMMENDED WEBSITES

**Clemson University Vehicular Electronics Laboratory** <http://www.cvel.clemson.edu/emc/index.html>

**Doug Smith** <http://emcesd.com>

**EMC Information Centre (Archived)** <http://www.compliance-club.com>

**Henry Ott** <http://www.hottconsultants.com>

**In Compliance Magazine** <http://incompliancemag.com>

**IEEE EMC Society** <http://www.emcs.org>

**Interference Technology** <https://interferencetechnology.com>

**Keith Armstrong** <https://www.emcstandards.co.uk>

**Kenneth Wyatt** <http://www.emc-seminars.com>

**Patrick André** <http://andreconsulting.com>

**Silent Solutions** <http://www.silent-solutions.com/index.htm>

# **University of Missouri EMC Lab**

<https://emclab.mst.edu>

**University of Oklahoma EMC** <http://www.ou.edu/engineering/emc/>

**Van Doren Company** <http://www.emc-education.com>

# **►**LIST OF LINKEDIN GROUPS

- Aircraft and Spacecraft ESD/EMI/EMC Issues
- Automotive EMC Troubleshooting Experts
- Electromagnetic Compatibility Forum
- Electromagnetics and Spectrum Engineering Group
- EMC Electromagnetic Compatibility
- EMC Experts
- EMC Troubleshooters
- **ESD Experts**
- Signal & Power Integrity Community

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# 2018 EMC CONFERENCES

# IEEE CONFERENCES

**2018 Joint IEEE International Symposium on EMC and APEMC** May 14-17 Singapore Liu Enxiao, [liuex@ihpc.a-star.edu.sg](http://liuex@ihpc.a-star.edu.sg) Er Ping Li, [erpingli@ieee.org](mailto:erpingli@ieee.org)

**2018 IEEE Symposium on EMC, SI & PI** July 30-August 3 Long Beach, California Ray Adams, [r.k.adams@ieee.org](mailto:r.k.adams@ieee.org)

**2019 IEEE International Symposium on EMC, SI & PI** July 22-26 New Orleans, Louisiana Dennis Lewis, [dennis.m.lewis@boeing.com](mailto:dennis.m.lewis@boeing.com)

**2020 IEEE International Symposium on EMC, SI & PI** July 27-31 Reno, Nevada Darryl Ray, [darrylr16@yahoo.com](mailto:darrylr16%40yahoo.com?subject=)

# OTHER CONFERENCES (2018)

**The 20TH Annual DOD (E3) Program Review** May 7 – 11, 2018 Huntsville, Alabama [www.fbcinc.com/e/dode3/attendeereg.aspx](http://www.fbcinc.com/e/dode3/attendeereg.aspx)

**6TH Advanced Electromagnetics Symposium (AES 2018)** June 24 – July 1, 2018 Marseille Cruise [www.mysymposia.org/index.php/AES18/AES18#.](http://www.mysymposia.org/index.php/AES18/AES18#.WpBfDq2ZMUE) [WpBfDq2ZMUE](http://www.mysymposia.org/index.php/AES18/AES18#.WpBfDq2ZMUE)

**EMC Europe 2018** August 27 - 30, 2018 Amsterdam, The Netherlands [www.emceurope2018.org/#august-27-30-2018-beurs](http://www.emceurope2018.org/#august-27-30-2018-beurs-van-berlage-amsterdam-the-netherlands)[van-berlage-amsterdam-the-netherlands](http://www.emceurope2018.org/#august-27-30-2018-beurs-van-berlage-amsterdam-the-netherlands)

**EDI CON USA** October 17 - 19, 2018 Santa Clara, California [www.ediconusa.com/](http://www.ediconusa.com/)

**Automotive Test Expo 2018** October 23 – 25, 2018 Novi, Michigan [www.testing-expo.com/usa/en/](http://www.testing-expo.com/usa/en/) **EMC COMPO 2019**

October 21 – 23, 2019 Hangzhou, China [www.emccompo.org](http://www.emccompo.org)

# ITEM MEDIA WEBINAR

**EMC LIVE 2018** April 24 – 26, 2018 Online Webinar Conference www.emc.live

**EMC Live Bootcamp** November 14, 2018 Online Webinar Conference www.emc.live

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