low in conductivity, thereby constituting a transfer impedance to external surface currents. Apertures in equipment item enclosures consist of any non-conductive openings or slits that will allow a re-radiation of incident EMP energy within the enclosure.

General Hardening Guidelines

The following guidelines are presented to provide the designer with basic solutions when a vulnerability to EMP has been isolated. Careful analysis of each possible EMP penetration, along with testing of the final design, are ultimate requirements for assurance of EMP hardness without costly over-design.

1. Employ conductive metallic enclosures for equipment. Electrically bond all seams and minimize the dimensions of non-conductive openings.
2. Employ electrically sealed chambers behind displays or other interfaces that require large openings in the equipment enclosure. Place EMP protection devices, which are subject to radiating high voltage or current transients, in separate chambers bonded to exterior walls.
3. Employ close braid shields or continuous foil shields over interface wires that cannot be otherwise protected from EMP. Terminate all EMP shields at the periphere of enclosures. Use conductive backshells on connectors for shield termination.
4. Filter interface lines that do not operate in the EMP spectrum. Select filter designs that will not breakdown due to EMP transients.
5. Limit voltage or current parameters on interface lines that must operate in the EMP spectrum. Series or shunt resistors and zener diodes or transient suppressors can be used.
6. Isolate interface electronics from sensitive internal circuitry such as microprocessors or random accessor memories. Prevent internal enclosure ground loops from carrying bypassed EMP transients.
7. Avoid the use of MOS devices or latchup prone devices in interface circuits.
8. Where data upset cannot be tolerated, use twisted shielded pairs with high level common mode termination, redundant data transmission, or fiber optic links at interfaces.
9. Use spark gaps on RF antenna transmission lines that operate in the EMP spectrum.
10. Employ Faraday shielded transformers where transformers are necessary, such as audio or pulse interface lines.

In general, EMP protection should coordinate with good EMI, EMC, and EMV (lightning) designs. Measures that avoid separate treatments for similar transients are cost effective.

This article was prepared for ITEM 84 *by L. W. Pinkston, Electromagnetic Effects Engineering, Rockwell/Collins, Cedar Rapids, IA.*

EMP SUSCEPTIBILITY ANALYSIS

Introduction

Nuclear weapon generated electromagnetic pulse (EMP) fields can be a serious threat to electronic systems.

EMP fields incident on electronic systems interact with system enclosures, cabling and antennas producing transient voltages and currents at system interface pins and in interior circuits. The induced EMP transients may cause two types of detrimental responses—either upset or damage.

Upset is the generation of false signals which can cause a system to take undesired actions. Damage refers to the degradation of a component to the point where it can no longer meet its design function criteria.

The EMP voltages and currents (and their associated time behavior) must be known at the circuit level in order to perform circuit analysis. Often the EMP specification is given in what is called a pin specification, which is the worst-case EMP voltages and currents that may appear at any I/O pin. The pin specification usually is defined in terms of a Thevenin equivalent source with a specified frequency and time behavior applied between each I/O pin and the lowest impedance return. Also the EMP specification often includes a surface current requirement for system components (blackboxes). The effect of this current on the internal circuitry must be determined via a penetration and coupling analysis. Once the EMP-induced voltages are known, the susceptibility analysis can then be carried out.

EMP susceptibility analysis is the systematic process for determining the hardness of electronic circuits to EMP-induced transients.

Susceptibility analysis evaluates the relative hardness of system components and circuits to EMP-induced upset and damage. The concept of design margin (DM) is used as the relative measure of EMP hardness. The design margin is a measure of the ratio of the amplitude threshold level required to cause damage or upset to the specified EMP environment level. When the circuit or component degradation threshold exceeds the EMP threat level with an adequate margin, no further analysis or hardening action is necessary. If the EMP threat level is close to the minimum threshold, then more refined analysis or EMP hardening action is required. Components or circuits with an adequate design margin are designated Category 2. Those with an inadequate design margin are designated Category 1.

A susceptibility analysis consists of six phases which are: data collection, susceptibility screening, detailed analysis, vulnerability classification, EMP hardening, and determination of hardness margin reliabilities and confidence levels.

EMP Threat and Induced Transient Specification

The three significant EMP environments are high-altitude EMP (HEMP), near-surface-burst EMP (NSBEMP), and system-generated EMP (SGEMP). HEMP, which is the most common threat and the only one considered in this article, is an intense planewave electromagnetic pulsed field which reaches a peak field strength of 50 kV/m in a few nanoseconds and lasts approximately one microsecond.

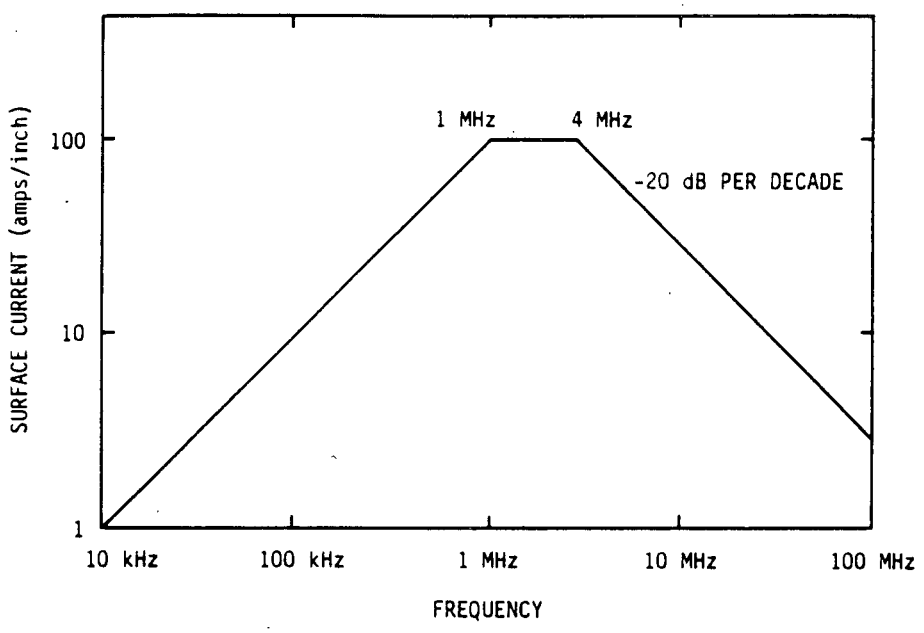


Figure 1. Example enclosure surface current specification.

HEMP is significant because a single high-altitude nuclear detonation can illuminate large geophysical areas with this intense field. All forms of EMP fields interact with system cabling, structures, and antennas inducing transient currents on conductors, including cables and equipment enclosures.

For many systems the EMP threat environment is specified by an enclosure surface current density specification and either a bulk cable current specification or a wire current specification. If not, then an EMP flowdown analysis must be performed to calculate these requirements from the specified free field.

An example enclosure surface current density specification is shown in Figure 1. It is necessary to perform an enclosure penetration and internal wiring coupling analysis to determine the current and voltage induced at interior or buried circuits.

An example bulk cable core current specification is a damped sine wave whose peak current is shown in Figure 2. The core current is specified to be the total common mode current on the cable core. In this example, the maximum voltage on each wire is taken to be limited to 1500V, and the individual wire currents are determined to be some fraction of the specified bulk cable current.

The wire or so-called pin transients are specified to be either a damped sine wave or a rectangular pulse having a short circuit current I(t) and an open circuit voltage V(t) or a source resistance R_s,

An example pin/wire transient specification is

$$V(t) = (300V)e^{-\pi ft/24} \sin(2\pi ft)$$

and

$$I(t) = I_o(f)e^{-\pi ft/24} (\sin 2\pi ft)$$

where $I_o(f)$ is shown in Figure 3 and f varies from 10 kHz to 100 MHz. The transient which is applied to each pin of an enclosure may have either initial polarity with current return through the lowest impedance return path.

Component and Equipment EMP Response

EMP produces two distinct kinds of equipment and piece part responses: upset and damage.

The spectrum of upset and damage thresholds for some generic piece part types are shown in Figure 4. As shown in the diagram semiconductors are very susceptible to EMP and thus frequently require protection.

Upset. Transient upset threshold is at least an order of magnitude below the damage threshold. It occurs when an induced EMP transient exceeds the operational signal level and has a time scale that falls within the circuit time response. As shown in Figure 5, an example of upset is the changing of state due to an EMP transient on the trigger input of logic circuits, or the drawing of an amplifier into saturation when the EMP transient is superimposed on its input signal.

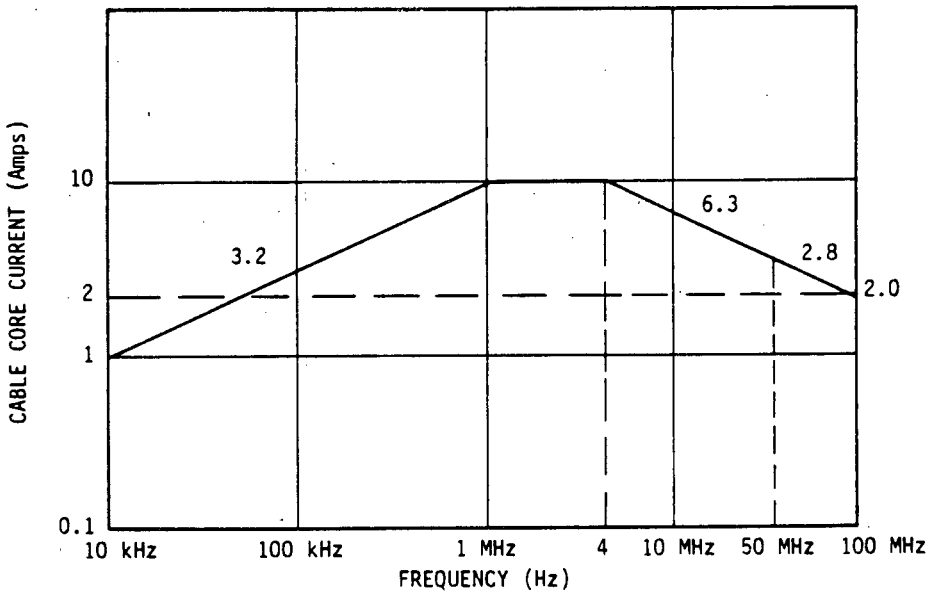


Figure 2. Example bulk cable core current specification.

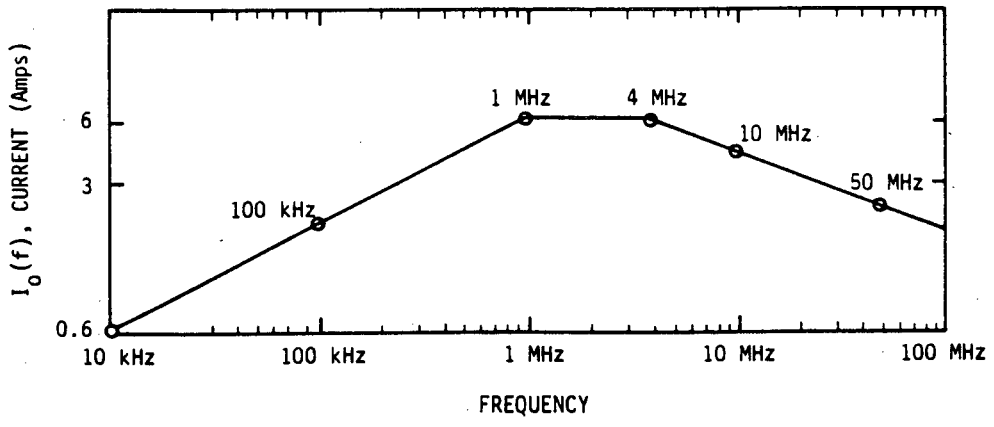


Figure 3. Example of amplitude-frequency plot for specified I/O pin short circuit current.

Another good example of operational upset is memory erasure or the loss of a clock or a synchronization signal. Depending upon the circuit function and design, loss of synchronization may be of little consequence for a short period of time. On the other hand, erasure of memory data may require reprogramming or reloading data. The outage time of a circuit is normally defined as the sum of transient disturbance time caused by EMP and the circuit or component recovery time. If this total time is less than that required to cause a system malfunction then the transient upset is not recognized.

Semiconductor Damage. Semiconductor junctions are vulnerable to thermal damage and electrical breakdowns when stressed by EMP transients. The most common failure is localized thermal runaway, which generally produces a resolidified melt channel across the junction, whose equivalent form is a resistive short circuit. Junction damage is most likely to occur when the EMP transient reverse biases the junction and drives it into second breakdown. Forward stressed junctions also fail but typically have damage thresholds which are three to ten times higher than reverse stressed junctions due to the low voltage and impedance levels present in forward conduction. For integrated circuits, metalization burnout and gate oxide breakdown (for MOS devices) are also prominent failure mechanisms.

Semiconductor failure thresholds for EMP transients can be predicted from known or measured data using models developed for discrete semiconductors and integrated circuits. These models, which are based on thermal considerations and experimental results, yield the following expression for the failure-threshold level,

$$P_F = k_1 t^{-k_2} \qquad \text{Equation 1}$$

where P_F is the power in watts required in a time, t in seconds, to produce device failure, and k_1 and k_2 are device-dependent constants.

For discrete devices, k_1 is usually determined by test and k_2 is unity for pulse widths less than 100 ns, 0.5 for 100 ns to 300 μs. Figure 6 illustrates the pulse width dependence of the failure power equation for discrete semiconductors. The

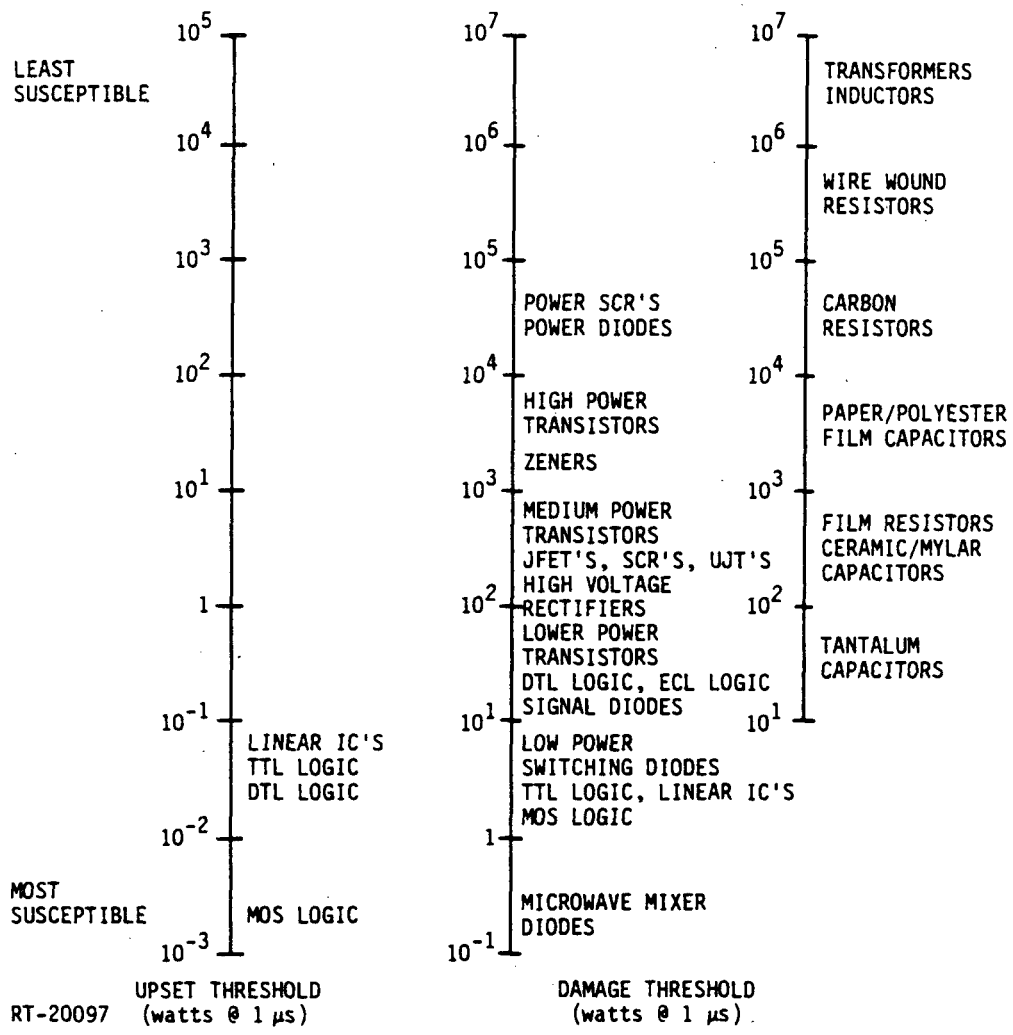


Figure 4. Spectrum of upset and damage thresholds of generic piece parts.

pulse widths for most EMP susceptibility analyses fall into the $t^{-1/2}$ regime yielding,

$$P_F = k\, t^{-1/2} \qquad \text{Equation 2}$$

where k is often called the Wunsch constant. As shown in Figure 6, Equation 2 provides a conservative prediction of failure power in the other failure regimes. Wunsch constants for some typical devices are given in Table 1.

Passive Component Damage. The passive components most susceptible to damage from EMP-induced transients are those with low voltage or power ratings and precision components where a small parameter change is significant.

Device	Type	k (w-sec$^{1/2}$)
1N750A	Zener	2.84
1N756	Zener	20.4
1N914	Diode	0.096
1N3600	Diode	0.18
1N4148	Diode	0.011
1N4003	Diode	2.2
2N918	Transistor	0.0086
2N2222	Transistor	0.11
2N2857	Transistor	0.0085
2N2907A	Transistor	0.1
2N3019	Transistor	0.44
2N3440	Transistor	1.1

Table 1. Wunsch Damage Constants for Some Transistors and Diodes.

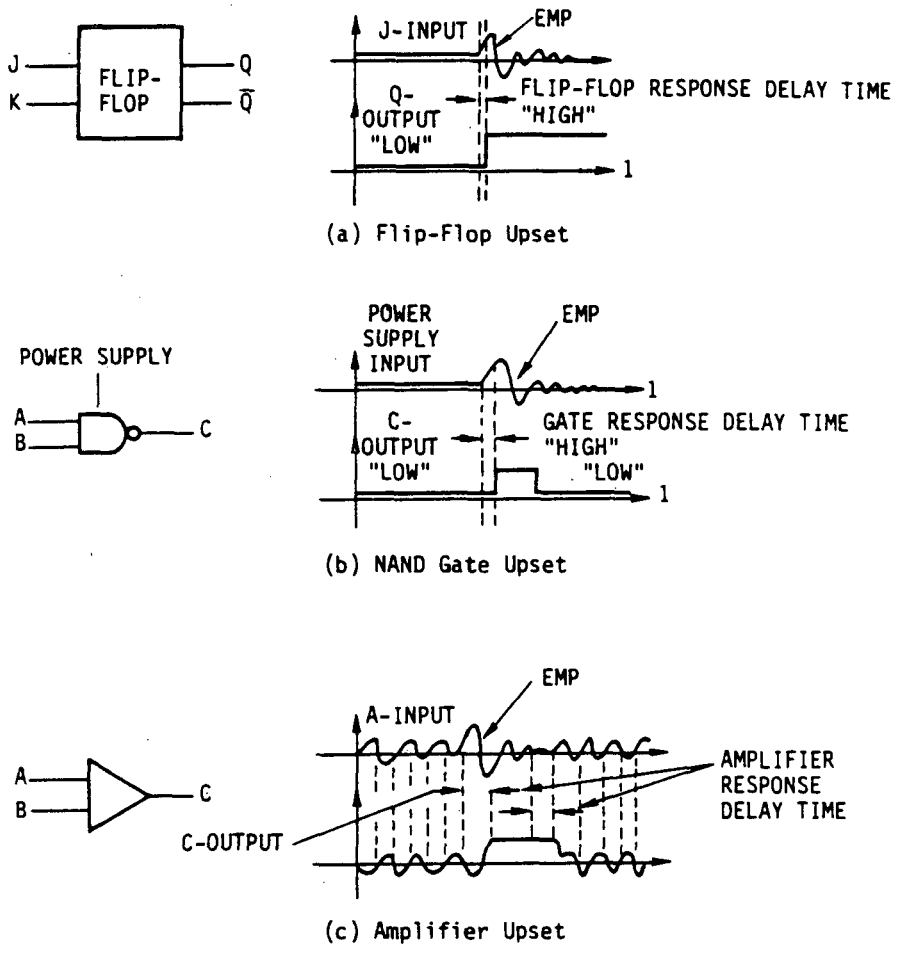


Figure 5. Circuit response to EMP.

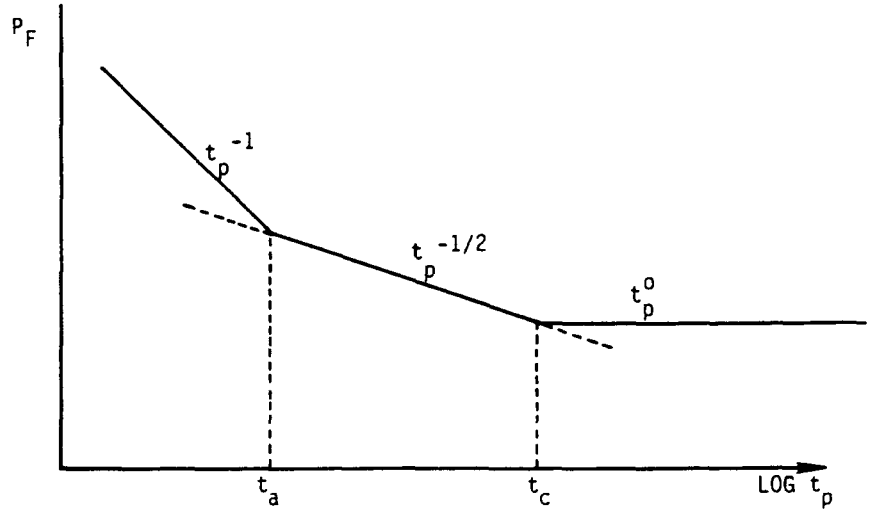


Figure 6. Pulse width dependence of the power required for semiconductor failure.

Resistors. Resistor failure due to EMP transients arise from electrothermal overstress and voltage breakdown. Resistors usually do not fail catastrophically but simply change resistance with increasing pulsed power. The failure threshold power for resistors is also given by Equation I where k_1 and k_2 are obtained experimentally.

Capacitors. Exposure of a capacitor to a transient current produces a voltage, V_c, across the capacitor which increases with time, as

$$V_c = \frac{1}{C}\int I dt.$$

For nonelectrolytic capacitors, this voltage increase continues until the capacitor's dielectric breakdown level is reached. For electrolytic capacitors, the voltage builds up in the same manner until the zener level of the dielectric is reached, at which time damage can occur.

Transformers, Coils, Switches and Relays. Damage to

transformers, coils, switch contacts, and relays from EMP transients occurs through electrical breakdowns of insulation, arcing across gaps and melting of wires. It may be possible for an EMP transient to initiate a breakdown path which is then sustained by normal operating levels.

Waveform Effects. The EMP transient appearing at the circuit level is usually not a rectangular pulse but instead is a complex waveform such as a damped sinewave. However, nearly all measured component failure data is obtained using rectangular pulses. Thus it is necessary to translate the rectangular pulse data to a form suitable for treating complex waveforms.

For more complex waveforms the following convolution integral must then be solved

$$k = \int_0^t P_{in}(t-\tau)\tau^{-1/2}d\tau,$$

where k is the rectangular pulse Wunsch constant, P_{in} is the time varying input power and τ is a dummy variable.

This convolutional approach does not lend itself to simple manual solutions for most waveforms. Thus simpler, less precise, translations are utilized. For the case of semiconductors stressed by damped sinewaves, rectangular pulse damage thresholds are transformed to those for damped sinewave inputs by the following pulse-to-frequency conversion

$$t_p = \frac{1}{2.25\ f}$$

where f is the damped sine frequency and t_p is the equivalent rectangular pulse duration.

Susceptibility Assessment Methodology

Determining the EMP survivability of a large system can be a difficult task. By using a systematic assessment methodology, the analysis can be achieved with reasonable expenditure of time and effort. The assessment method is described below.

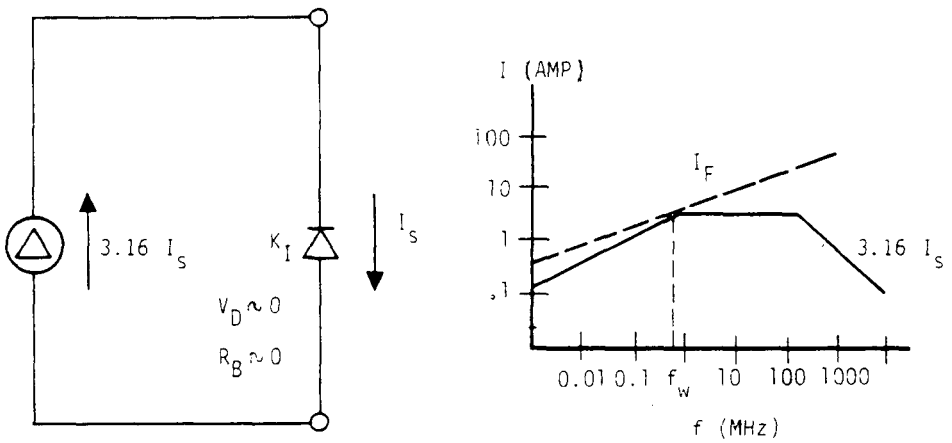
Data Collection. Data collection, an essential step in the assessment procedure, involves the acquisition of all technical documentation necessary for performing the analysis. The documentation to be obtained during this phase includes descriptions of the system's electrical and mechanical characteristics, operational modes, performance criteria and the values of the components damage constants.

Susceptibility Screening. Circuit screening is a rapid means of performing a preliminary susceptibility analysis capable of identifying major portions of subsystem circuits inherently hard to the EMP-induced transient.

The circuit screening criteria are simply determined by deriving the worst-case relationship between the key failure parameters of components and the specified levels of EMP-induced transients. Screening criteria must be developed for all important active and passive components in the subsystems. An example derivation of failure criteria for a semiconductor screen is shown in Figure 7.

An initial screen based on generic part type is performed on system circuits to eliminate well-established intrinsically hard components. The generic screen is based on the induced transient levels, circuit component location, component generic type, and associated level of EMP hardness.

A screen of interface circuits is performed next. These I/O circuits are most susceptible to damage or upset since they are directly exposed to the EMP pin/wire interface voltage and current.



$$3.16\ I_S = I_F = (1.5)\ (k/V_{BD})f_w^{\frac{1}{2}}$$

$$k = (3.16/1.5)I_S\ V_{BD}f_w^{-\frac{1}{2}}$$

Figure 7. Sample derivation for semiconductor damage.

The screening procedure involves the determination of the potentially vulnerable components in the interface circuits; establishing the components threshold factors (k, voltage breakdown, critical resistance) and the comparison of the threshold factors with the screening criteria. Circuits containing components that pass all the screening criteria are designated Category 2 and require no further analysis. The circuits with components that fail one or more of the screening criteria are designated Category 1 and require detailed analysis.

Buried circuits are also screened and categorized during the assessment. Buried circuits are all the circuits which are not directly connected to I/O pins.

The buried circuit screening procedure is similar to that for interface circuits. Each buried circuit is examined for potentially vulnerable components and the appropriate damage factors are determined. The EMP coupling modes and coupling parameters are estimated from the connecting wiring configuration. The vulnerable components are then screened using the buried circuit screening criteria. Finally, circuits are classified Category 1 or 2, depending on the screening outcome.

Detailed Analysis. Detailed analysis is performed on all of the Category 1 circuits. Detailed analysis methods utilize both hand and computer-aided analytical tools. Hand analysis is carried out through standard analytical means using equiva-

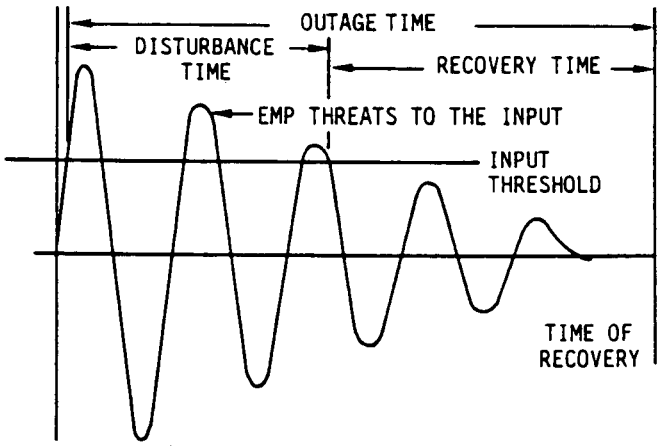


Figure 8. Circuit outage time, T_o.

Device Type	Clamping (or Filtering) Thresholds	Operate Time (s)	Highest Burnout Energy Threshold (J)	Shunt Capacitance (F)	Typical Circuit Applications	Possible Disadvantages
Varistors						
MOV	40-1500 V	$<10^{-9}$	$<10^{3}$	10^{-9}	Power,AF	High capacitance
Semiconductors						
Forward diodes	0.2-0.6 V	$<10^{-9}$	$<10^{1}$	10^{-12}	AF,RF	Low burnout energy
Breakdown diodes	2-200 V	$<10^{-9}$	$<10^{2}$	10^{-8}	Power,AF	High capacitance
Spark Gaps						
High-speed gaps	550-20,000 V	$<10^{-9}$	$<10^{3}$	10^{-11}	Term,AF,RF	Power-follow, high cost
Arresters Using High-Speed Gaps	550-20,000 V	$<10^{-9}$	$<10^{3}$	10^{-11}	Power	High cost
Filters						
Ferrite chokes, beads	RF	—	—	—	Power,AF	Ineffective protection, DC saturation
Feedthrough capacitors	RF	—	—	—	Power,AF	Dielectric breakdown
General RLC circuits	DC,AF,RF	—	—	—	Power,AF,RF	Impedance mismatching

Table 2. Comparison of Protection Devices.

lent pulse or CW excitations and linear analysis techniques such as Kirchoff loop and nodal equations, Laplace transforms, and AC analysis—whichever is appropriate for the particular circuit.

More complex circuits utilize computer-aided analysis and employ one of several available analysis computer programs. At IRT these include the following codes: AC-CODED, CIRCUS, SCEPTRE, SPICE, SYSCAP, and TRAC.

Circuits found to be category 2 by detailed analysis require no further action. Circuits determined to be category 1 require hardening or test.

Upset Analysis. Upset analysis determines upset thresholds for all circuits that could cause an outage of critical output functions (COF) or buried critical functions (BCF) for an unacceptable period of time.

The circuit outage time, as shown in Figure 8, is compared to the maximum allowable outage time T_A. If the COF or BCF circuit outage time is less than one-third the allowable outage time the circuit is categorized as Category 2 and requires no further consideration. However, if the COF or BCF circuit T_o is greater than $T_A/3$ the circuit is categorized as Category 1 and requires EMP hardening or test.

Vulnerability Classification. The objective of the detailed analysis is to establish the EMP design margin for each circuit analyzed. The EMP design margin (DM) for damage is

$$DM = 20 \log_{10}(X_I/X_F) \qquad \text{Equation 3}$$

where

X_I = induced EMP voltage or current
X_F = the failure voltage or current.

The design margin for COF or BCF upset is

$$DM_T = 20 \log_{10}(T_A/T_o) \qquad \text{Equation 4}$$

where

T_A = maximum allowable outage time
T_o = circuit outage time.

For example consider the case where circuits determined to have a damage $DM_T \geq 10$ dB outage time upset $DM_T \geq 10$ dB, are classified as Category 2 (i.e., hard) and require no further consideration. Circuits determined to have a damage DM < 10 dB or an outage time upset $DM_T < 10$ dB are specified Category 1 circuits and require hardening or test. The Category 1 circuits may be divided into two classes which are: medium ($0 \text{ dB} \leq DM < 10$ dB) and soft ($DM < 0$ dB). The medium circuits are candidates for tests or hardening, whereas EMP hardening techniques must be implemented for all soft circuits. Some of the factors to be considered before circuits or components are recommended for tests are: cost of hardening versus cost of test, impact on schedules, test complexity, the required test facilities and their availability. In addition, Category 1 components or circuits require hardness assurance control throughout production and deployment which drive up the life cycle costs.

EMP Hardening. EMP hardening at the circuit level utilizes either protection devices or transient tolerant designs.

EMP protection devices operate predominately in one of two ways: by clamping (limiting the magnitude of currents or voltages) or by filtering (removing energy in certain frequency bands). The important characteristics of some EMP protection devices are shown in Table 2.

Practical clamping devices for EMP protection, which are generally placed in shunt with the input lines, include a metal oxide varistor, diodes, and spark gaps. Clamping devices appear as a high-resistance shunt until the device threshold is reached, at which time the device becomes a low impedance path and voltage is either clamped near the threshold point (varistor, diode) or drops to a lower value (spark gap).

A filter suppresses certain frequency components from an EMP surge, thereby reducing the energy that sensitive piece parts must withstand. Clamping devices operate only above a specified magnitude of surge voltage, but filters respond to specific frequencies regardless of magnitude. They can thus suppress spurious frequencies that might cause system upset, even if the interfering transient is not strong enough to activate a clamping device.

Devices used to implement transient protection must be rugged enough to withstand the transient and must be compatible with circuit operation. Some of the more important considerations are: maximum operational voltage excursion, bandwidth or bit rate, allowable capacitive load, circuit function and the induced EMP waveform.

Transient tolerant designs fall into three categories: hardware, software, and procedural. Hardware design techniques are useful for hardening against component damage and circuit upset, whereas software and procedural techniques are only useful for hardening against EMP upset.

Transient tolerant hardware design techniques consist of using circuit components such as relays (without suppression diodes), transformers, optical isolators, series bifilar chokes and redundant system elements.

Software hardening measures are most useful for computer elements. For example, the use of plausibility checks on data is quite mundane, yet very effective as a means of "filtering" data made erroneous by EMP-induced upsets.

Another hardening measure, called checkpoint and rollback (CPRB) provides a means of tolerating logic upsets due to EMP.

Error detecting and correcting (EDC) codes can be an effective hardening measure against EMP-induced upsets by allowing toleration of data errors caused by these upsets.

All of the hardening measures discussed above involve hardware or software implementations. To support these measures EMP operational procedures should be instituted for the day-to-day operation of the system. The operational and maintenance staff should be educated on the system effects arising from EMP transients. Operational procedures should be developed to recognize and recover from these effects when they occur.

This article was prepared for ITEM '84 *by Marion A. Rose and Lloyd Duncan, IRT Corporation, San Diego, CA.*