INTRODUCTION

With the growing awareness that most electronic systems essential to national security must function properly during and after exposure to a nuclear environment, many prime system procurement agencies now include radiation requirements as part of their system specifications. This implies a new facet to be considered by a contractor during the system design and development. Several aspects of the radiation-hardening problem are relatively unique, such as added program costs to achieve protection and extreme engineering difficulties encountered in subsystem- or system-level design.

A specific characteristic of the hostile nuclear environment is the multiplicity of kill mechanisms. Photon pulses can produce both current transients and catastrophic failures; device surface degradation modes can be caused by the ionizing dose deposited by the total radiation environment; and neutrons produce desirable changes in electronic parts characteristics.

An electromagnetic pulse (EMP) is another one of the products of a nuclear detonation. It presents a threat to electrical components since its presence can disable or cause malfuntions in electronic equipment.

Currents induced on a system's interconnecting cables by the effects of EMP are known to produce extraordinarily large transient signals at electrical interfaces. Such transients can cause functional upset of internal electronics and, if they contain sufficient energy, could result in piece-part destruction. It is therefore essential to determine the response of vulnerable piece parts and related circuits to any induced overstress signall; i.e., a susceptability analysismust be performed. The primary goals of the susceptability analysis must establish if sufficient pulse energy is available to induce either upset or burnout, and to recommend methods of protecting circuitry against these undesirable effects.

Performance of a good susceptibility analysis involves several phases of investigation as diagrammed in Figure 1. A typical program begins with a review of the system design to establish any potential upset and burnout paths, to select the most sensitive circuits, and to eliminate inherently "hard" designs from futher investigation. The second phase is the performance of a detailed analysis on the selected circuits and the determination of the applied energy to known sensitive parts within the circuit. The step normally involves modeling the circuit, deriving transfer relationships, and generating response expressions for each unique circuit. The third and most important phase involves the determination of the circuit's response and data obtained in this portion of the program provides answers to the following questions. Does the induced signal upset the circuit function? If so, for how long? Will the induced current pulse cause permanent damage to a part within the circuit? The fourth phase of the analysis involves the assessment of the overall effect on the system based on the individual circuit response to the induced current pulse. The fifth and final phase of the susceptability analysis is the development of methods of protecting vulnerable circuits against the transient surges. This step may require not only a reiteration of the earlier analysis of the circuit for survivability, but also additional investigations to establish its ability to meet original operation specifications with the added protective measures.

SELECTING SUSCEPTIBLE CIRCUITS

The first step in performing a susceptibility analysis on a system is the categorization of the critical or vulnerable circuits. Decisions made at this point are frequently based on system effects generated by circuit failures. For example, a solenoid driver may be momentarily activated without detrimental system effect because of solenoid response time, while it would not tolerate a permanent device failure. All interface circuits are reviewed first, and those which have signal-attenuating components between an input/output pin and a sensitive amplifying device would normally receive low-priority interest. Attenuating piece parts are usually passive components such as resistors, capacitors, or inductors whose position in the circuit topology would cause much of the energy from the applied pulse to be reduced to a significant degree. It is frequently necessary to determine the circuit's frequency response because this may affect its susceptability to the induced signal. Those circuits whose bandwidth does not include the EMP frequencies may usually be excluded from further analysis.

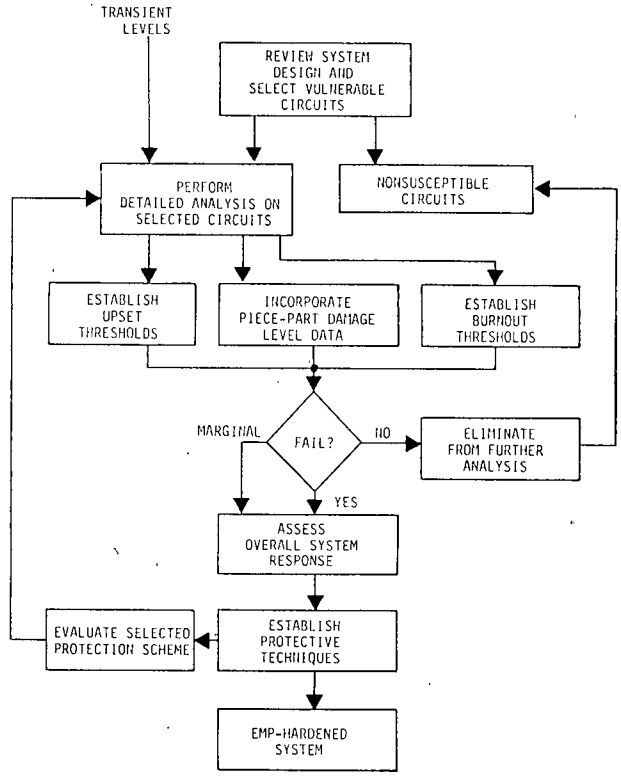

Figure 1. Flow diagram of a typical EMP susceptibility program.

In addition to the investigation of the interface circuit itself, it is often necessary to examine related internal circuits. It is possible for such contemporary circuits to be overstressed when an interface circuit breaks down and subsequently transmits energy to them. This is normally dependent on the type of semiconductor involved in the interface network. Power devices, because of their junction areas, can dissipate a higher-energy pulse than small signal devices or integrated circuits. Therefore, when discrete power semiconductors are used in a design, the resultant circuit is usually less susceptible than one which employs integrated circuits. This fact is illustrated in the susceptibility spectrum of Figure 2. In some cases, it may be necessary to determine the effect of stray electrical characteristics such as capacitance in physical patterns of a printed circuit board or the lead lengths of components. Such parameters may significantly affect the energy delivered to a sensitive circuit element.

Decision techniques employed during this review are normally dependent on the modes of failure that are under study, i.e., upset, burnout, and the associated system effect. The consequence that should come from this initial review is the elimination of as many circuits as possible from further study without jeopardizing the confidence of the analysis program.

ANALYTICAL PROCEDURES AND TOOLS

Susceptability analyses of circuits are performed to determine whether the level of the applied stress is sufficient to cause circuit upset and/or damage to sensitive circuit elements. Upset is defined as a drastic alteration of a circuit's normal operating condition to some extreme condition (e.g., saturation or cut-off of a transistor), resulting in a significant change at the circuit's output. Damage, on the other hand, refers to permanent detrimental changes in device characteristics.

The analysis sequence usually consists of the following steps. The actual methods by which these steps are carried out include simple hand analysis, as well as more sophisticated approaches utilizing various transient analysis computer codes.

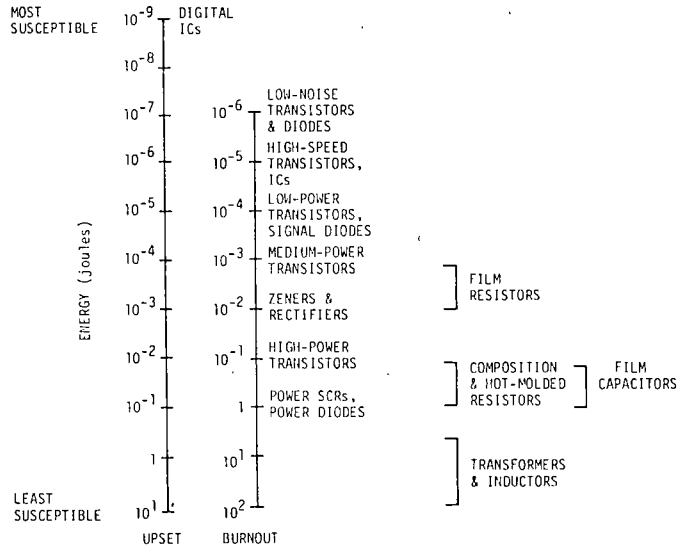

Figure 2. Typical ranges of upset and burnout energies for various circuit elements (pulse widths in the microsecond region).

1. An equivalent source representation is determined for the induced waveform. The complex representations required for the EMP/SGEMP*-induced currents usually presents little difficulty for computer analysis. For hand analysis, however, crude approximations are often required. The usual approach in this case is to characterize the complex waveform by one or more square pulses whose total energy equals the energy in the waveform and whose amplitudes are related in some manner to the waveform's amplitude profile.
2. The probable points of entry into the circuit of the EMP/SGEMP waveform are then identified. Any input/output and power supply lines are the most likely penetration points. In addition, it is frequently necessary to investigate second-tier circuits (second circuit in from input or output of a box) which may be much more sensitive and may burn out if the primary interface circuits break down or malfunction and apply electrical surges to the second-tier circuits.
3. The transfer functions from the entry points to specific devices are calculated, yielding the EMP/SGEMP-induced current levels at the device terminals. Since the EMP/SGEMP waveform generally is a transient signal whose width is in the microsecond ranges, this step requires that the high-frequency and transient response of the circuit elements be taken into account.
4. Next, the upset level for the circuit and the estimated or measured damage threshold of the devices of the circuit are established. Semi-conductors are considered first because they are the circuit elements most likely to be damaged by transient energy. This will be discussed in more detail when analytical damage points are examined.
5. The final step in the analysis is to assess the susceptibility of the circuit and circuit elements by comparing the EMP/SGEMP-induced signal levels with he level determined to cause upset and device damage. A desirable safety margin usually exists when the expected EMP/SGEMP level is an order of magnitude less than the calculated upset and/or damage threshold level.

Available analytical techniques are divided into two categories: (1) hand analysis, incorporating textbook procedures useful for "rough" circuit susceptibility approximations, or for evaluating the response of simple circuits, and (2) computer-aided analysis for detailed evaluation of complex circuits, for studies requiring time histories of response, or for very accurate numerical determinations. The method is chosen primarily on the judgement of the analyst but is usually based on desired accuracy, complexity of the circuit, failure mode of interest, and allotted budget to complete the analysis.

*System Generated EMP

Representative computer programs used in support of analysis work are TRAC [1] and SCEPTRE[2]. These are highly efficient digital computer programs which employ Ebers-Moll, charge control, Linvill-lumped, and linear models for semiconductor simulation. These codes have the capability of analyzing circuits which employ semiconductors such as bipolar transistors, JFETS, MOSFETS, diodes, zener diodes, and operational amplifiers.

Adaptations of these computer circuit analysis codes are used to understand and evaluate burnout and transient (upset) effects in electronic circuits due to EMP/SGEMP-induced currents. The computer program selected for a given analysis is determined by th circuit topology and driving stimulus. The circuit is modeled according to the related computer code. This complex model is then driven by the appropriate voltage and current generators representing the signal contribution from the induced currents. The computer code finally determines the available energy in the selected areas of the circuit which allows the analyst to ascertain if an upset or burnout condition exists in the circuit.

DETERMINING SUSCEPTIBILITY

Two primary effects must be determined from the analytical evaluation. These are (1) will the device or circuit upset, or (2) will the device or circuit be seriously damaged, i.e., burned out? Upsets may occur anywhere in the system as a result of integrated circuits and discrete component circuits responding to the induced signal. Generally, upset level cannot be directly determined from a manufacturer's or designer's specification and, therefore, is included as part of the analysis task.

Upsets resulting from an EMP/SGEMP-induced signal are transient in nature and produce states which alter the operating conditions of affected circuits. While these states do not permanently impair an individual part's operation, they may have a much greater significance on the system performance.

Consider upset effects on airborne or satellite applications; if a circuit upset is such that some irreversible action is initiated and this action, in turn, causes degradation of the mission or complete mission failure, corrective action should be taken. If such an upset occurs in the memory of a satellite's computer, for example, and the memory can be corrected by ground command within allowable time allotments, then perhaps no remedial action is necessary. Upsets that do not cause irreversible actions, such as momentary power supply fluctuations, can usually be ignored.

Therefore, to assess the impact of an upset, both the condition of upset and the resulting system response must be established. Determining the condition for component upset may be as simple as comparing the voltage generated by the energy pulse with the manufacturer's specification. However, this is seldom the case, since the response of the circuit or component must be determined for the very short time span of the induced signal. In addition, concurrent effects on associated circuits and parts must be considered. After the proper conditions for an upset state have been established, the next step in the assessment is to evaluate the overall impact on the system. An upset in the system is normally considered as any response which is other than the prescribed performance. This is usually viewed as an undesired change in signal characteristics. These include voltage and current levels, transmission or reception strengths, or improper control of other related systems. Here, also, the response of the system must be considered since microsecond upsets will have no effect on millisecond response circuits. In addition, the concurrent state of other circuits must be considered. Upsets may be widely categorized as those in digital circuits and those in linear circuits. Table 1 gives examples of the most frequently observed system effects and some of the circuit types contributing to them.

Permanent damage is the second mechanism of susceptibility and will primarily affect semiconductor elements, although passive components may be damaged if the pulse energy is sufficiently large. Semiconductor junctions and metalization systems are very vulnerable to thermal damage and breakdown when stressed by transient electrical energy. Assessment of damage is based on actual test data or empirical relationships derived by the analyst.

Junction damage occurs as a resolidified melt channel across a junction whose equivalent electrical form is a resistive short circuit. Damage to reverse-biased junctions is generally the result of thermal-mode "second breakdown" which arises from local thermal runaway effects induced by a severe current concentration within the junction area. Forward-biased junctions are also damaged by localized thermal runaway; however, the second breakdown phenomenon will not be observed due to a low impedance level already present in the forward condition. Interface breakdown is a damage mode frequently observed in monolithic microcircuits and appears electrically as resistive shunting paths between adjacent metalization stripes. It is caused by electrical breakdown paths being formed across the silicon substrate surface between the metalization stripes. Device metalization damage is caused by Joule heating, and is observed as melting, splattering, and open-circuiting of the internal interconnection system.

All of these damage mechanisms are energy-dependent processes, since they are associated with some form of thermal failure. In general, interface breakdown and device metalization damage usually occur at energy levels in excess of those required to cause significant junction damage in typical semiconductor devices. Forward-stressed junctions typically have higher damage thresholds than reverse-stressed junctions, due to the low voltage and impedance levels present in forward conduction. It should be noted that normal electrical bias conditions do not significantly change the damage threshold level of a device in a circuit. Piece-part specifications cannot be relied upon for prevailing characteristics during breakdown since they control parameters useful only when maximum ratings have not been exceeded.

DAMAGE THRESHOLDS OF CIRCUIT COMPONENTS

Extensive studies and experiments[3-5] have been carried out for the purpose of developing a criterion for predicting threshold failure levels in semiconductor devices from known or measurable quantities. Researchers have derived a suitable criterion, based on thermal consideration, along with experimental results. This criterion is expressed in terms of a semiempirical expression, which is

$$p = K/t^m$$

where P is the power dissipation in a junction required in time t to produce failure, K is a device-dependent constant which changes with the time regime, and m is 1 for 10-to 100-nsec pulse widths, 1/2 for 100-nsec to 50-usec pulse widths, and 0 for longer pulses. Table 2 lists the values of K for some selected semiconductor discrete devices. These constants are conservative values representing the lowest points at which burnout has been observed. K values for a specific JEDEC device may vary as much as an order of magnitude due to such factors as difference in manufacturing processes or temperature gradients. Hence, part type calculations with selected K values must have appropriate safety factors included to account for this variation.

Test data on the transient damage threshold of passive components is very limited at the present time. The passive components which are most susceptible to damage, of course, are those with very low power or voltage ratings, or precision components in which a small parameter change is significant. Permanent damage to passive components usually results from localized Joule heating. Voltage breakdown is a problem with capacitors and transformers; however, no significant permanent damage generally occurs except for capacitors where there is very low impedances between them and a dc supply in a circuit's topology. Resistor damage generally arises from localized heating of the resistive element (hot-spotting) leading to thermal destruction of the resistive matrix and insulation jacket. Composition resistors have transient damage thresholds on the order of 10^3 to 10^4 times their average power rating.

SUSCEPTIBILITY ASSESSMENT AND REDUCTION

Application of the upset or damage information then permits the assessment to be finalized and a susceptibility prediction formulated. From this prediction, it may be concluded at what level a failure will occur and the mode of failure. The next step in the evaluation sequence is to assess the effect of the damage on system operation.

Table 1.

	Functional Effect	Produced by upset of:
I.	DIGITAL CIRCUIT UPSETS	
1.	Changes in command functions	Flip-flops, discrete circuits
2.	Alteration of stored information	Registers, memory elements
3.	Changes in system timing	Clocks, counters, oscillators
4.	Changes in drive states	Logic buffers, interface circuits
5.	Changes in processing states registers	Non-synchronous logic
II.	LINEAR CIRCUIT UPSETS	
1.	Changes in signal level	Amplifiers - ac/dc
2.	Loss of regulation	Voltage and current sources
3.	Loss of synchronous states	Phase-lock circuits
4.	Control instability	Servomechanisms
5.	Loss of information in process	Demodulators, choppers, amplifiers
6.	Premature activation/ functional loss of protective circuits	Power supply "crowbars" and current limiting circuits
7.	Loss of signal generation	Sinusoidal oscillators, dc-dc inverters, dc-ac converters
8.	Improper wave shapes	Active, passive filter networks

Table 2. Typical K Values for Various Devices

Device	Type	K ($W\text{-}sec^{1/2}$)
1N746	Zener	1.1
1N914	Diode	0.85
1N3051B	Diode	1.9
1N3600	Diode	0.18
2N1132	Transistor	0.23
2N685	SCR	1.4
2N1596	SCR	0.94
2N2102	Transistor	0.77
2N2222A	Transistor	0.1
2N490	Unijunction	1.0
2N2346	SCR	3.2
2N2907A	Trans	0.1

In most cases, a burnout of a piece part will lead to a disabled circuit and quite possibly to failure of either whole or part of a mission, should the application fall in the realm of airborne or space equipment. If such damage is identified through analysis, measures should be taken to either redesign the circuit to remove the problem or to add appropriate protective devices. In a very few cases, it may be possible for a mission or function to be accomplished at a less efficient level when damage takes place. But, even here, it is dangerous to allow the possibility of such a situation to exist. The conclusion must be that each failure mode should be examined in the light of its effect on system operation and corrective action taken where clearly necessary.

Methods are available for mitigating the effects of the electrical moise transients for which the susceptibility analyses are performed. These are based on (1) limiting the EMP signal to a level which assures no damage to the circuit components, (2) using the fundamental differences between noise and signal to prevent circuit malfunction, or (3) a combination of both. The necessity to protect against damage will normally exist for all mission-critical circuits of a system. Temporary circuit malfunction may, however, be acceptable in many cases.

If protection against circuit malfunction or upset is required, the differences between noise and signal can be used to discriminate against the noise. In most cases, an existing or planned circuit design will not initially include provision for doing this; e.g., a digital interface circuit may response to any signal whose amplitude is above a threshold level for some specific time duration. As the time duration decreases, the threshold voltage will increase as shown in Figure 3.

A coupling analysis or test may show that noise pulses sufficient to reach into the response region will exist for the specified environment. Modification of the circuit will then be required. For example, if the normal signal is of very long duration, a pulse width discriminator can be added such that pulses of duration less than $\tau_{p(MIN)}$(greater than the noise duration) will be ignored completely. The circuit response would then appear as diagrammed in Figure 4.

If the interface is not amenable to this particular form of discrimination, because of a high data rate and/or short normal pulse duration, then some other form of discrimination may be used. Pulse-code modulation and phasing with respect to a reference signal are examples of techniques that can be used to reduce the probability of interpreting noise as signal to an acceptably low level. Analogous techniques are applicable to ac signals; i.e., the normal signal frequency may be significantly removed from the predicted and/or measured noise spectrum. An ideal filter would completely remove the noise, precluding both circuit upset and damage. Practical filters can reduce the noise to a tolerable level except where the noise and signal frequencies are too close together. In such cases, use can be made of the transient nature of the noise, random phrasing, etc., to prevent circuit or system malfunction. Finally, at the system level, techniques comparable to circumvention may be used. These are based on detecting, in some way, the presence of the environment which produces the noise, assuming that any state change coincident with or shortly following the environment is possibly erroneous, and restoring the system state to that which existed preceding the noise. Circumvention is an extreme solution usually required in a very special cases.

Noise signals may also reach a level which cause damage to circuit components, principally burnout due to excessive energy deposition in a time short compared to thermal time constants. The use of filters, as mentioned above, is a useful technique for reducing this energy deposition in some cases, but some form of signal amplitude-limiting will generally be required as well. This technique involves the use of electronic surge arrestors (ESA), zener diodes, etc., to clamp the input voltage at a level somewhat above the maximum normal signal level. Normal circuit operation is not altered, but overvoltage/overcurrent conditions are consequently minimized. Zener diodes are especially useful at the blackbox level, while ESAs are more useful for very long cable runs between ground facilities and must frequently be supplemented by zeners at the circuit input level. The ideal response of such clamping devices would be to have them turn on instantaneously when the input exceeded the clamping level, hold exactly the clamping level throughout the noise pulse, and return to the non-conducting state instantaneously at the end of the pulse. Practical devices, of course, have finite turn-on/turn-off times, non-ideal V-I curves, and inherent packaging constraints. As a result, short-duration (or high-frequency ac) pulses of up to a few times the nominal clamping level may still appear at the circuit input at very high surge currents. If these are of sufficient amplitude to result in circuit damage, additional filtering will be necessary to reduce the noise to an acceptable level.

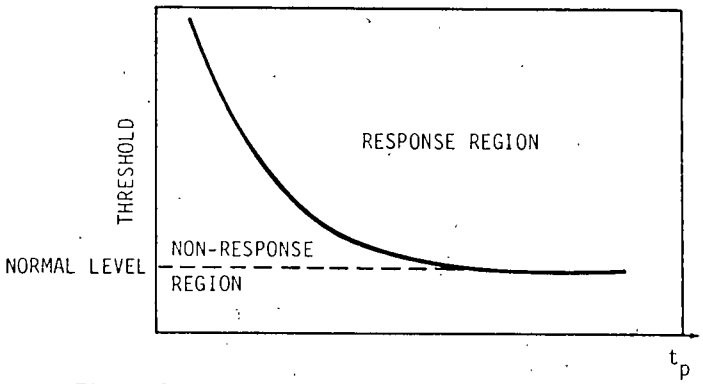

Figure 3. Typical variation of circuit threshold with pulse duration.

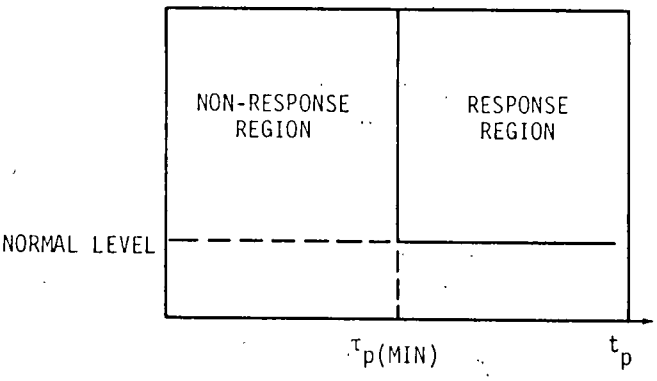

Figure 4. Modified threshold variation.

COMBINED ENVIRONMENTAL EFFECTS

The emphasis in this article has been on objectives and techniques of performing a susceptibility analysis and has essentially addressed only the effect of EMP/SGEMP-induced signals. It is frequently both impossible and inaccurate to isolate these effects since other factors of a nuclear environment may be generating simultaneous effects. One of the primary multiple effects is the EMP signal which has coupled on interconnecting wires, combined with the signal induced by the internal EMP (IEMP) inside the box. Also, the EMP field external to a system must include the system-generated EMP (SGEMP) which will affect the induced signal on the interconnecting wiring. A third multiple effect is that produced by the ionizing portion of a nuclear environment combined with the effect of an EMP/SGEMP-induced signal. Ionizing radiation will typically introduce transient perturbations in semiconductors by totally or partially ionizing the silicon or germanium materials. This, in turn, both upsets the established states and alters the impedance levels represented by semiconductor junctions. Response of a circuit or part to a simultaneous application of an EMP/SGEMP high-energy pulse, when the circuit or part is in this ionized condition, will certainly differ from the predicted response when the part or circuit is not so ionized. Therefore, it is frequently necessary to consider these potentially synergistic effects when executing an analysis, since addressing the independent effects could result in erroneous conclusions.

These combined effects are pointed out only as items which must be considered when performing a susceptibility analysis. A full discussion of all these combined effects and the conditions of multiple exposure are beyond the scope of this article, but are frequently environmental conditions which must be determined to meet the goals of a total EMP susceptibility program.

IN-HOUSE OR SUBCONTRACT?

For the system's designer, the preparation and conduct of a good EMP susceptibility program is usually beyond his capability, experience, scheduling, and financial considerations. When the need for EMP or nuclear hardening program development arises, the majority of companies involved in equipment design for military use rely on consultants in the field of radiation effects on electronics and materials.

From a financial viewpoint, most firms concerned with producing military electronic systems do not maintain staffs for EMP analyses or test facilities, unless all their products must be qualified to withstand some aspect of the nuclear threat. Personnel involved with a system's mechanical and electrical construction can be made aware of the basic EMP problems produced by a nuclear environment, and subsequently include some protective measures in their designs; however, the educational time span needed to cover the multi-facet EMP problem is normally too long when a system's developmental schedule is considered. As a result, one important task assumed by an EMP subcontractor is the compilation of applicable design guidelines for the specific threat levels. This insures the production of a non-susceptible design during the conceptual phases of a system's development, and frees the equipment designer to deal with the basic operational problems.

When the combined environment problems are considered, the need for consultation services becomes essential to the system's designer, as he must now deal with all facets of the nuclear threat, including EMP. Many solutions for the effects of EMP on electronics and materials only inhance the problems caused by the other products of a nuclear detonation, and vice versa.

As in all hardening programs, the emphasis must be placed on early design consideration, taking into account the circuit and system's response to the nuclear threat. Only by early design considerations can costly redesign be avoided.

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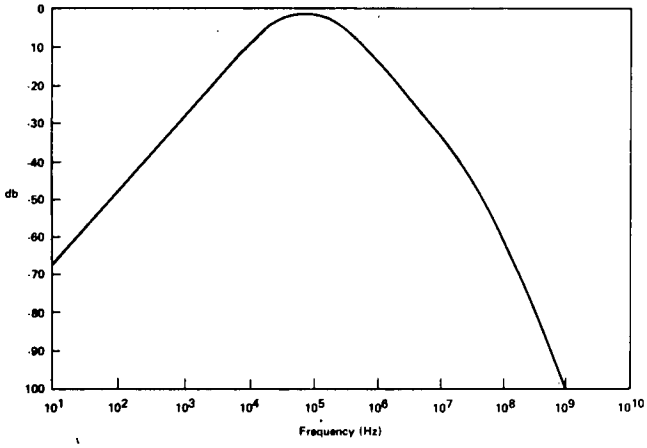
SUPPRESSING CONDUCTED EMP TRANSIENTS

EMP POWER & SPECTRUM

EMP pulses are characterized not only by high intensity but also by a broad range in the electromagnetic spectrum. RF energy produced in nuclear blasts span the range from commercial radio up through radar frequencies. This peaks out at about 100kHz and drops off substantially at 1GHz as shown in Figure 1.[2] Most military and commercial communication and radar equipment operate within this range.

Some components, such as vacuum tubes, resistors and capacitors, are relatively hard. However, semiconductors are quite sensitive to the fast electrical pulses generated by EMP. Burn-out levels for transistors, diodes, and ICs cover a broad range. Minimum observed energy levels to cause destructive effects occur as low as 10^{-7} joules for microwave diodes up to 10^{-1} joules for some audio transistors. Contrary to logical thinking, steady state power dissipation may not be indicative of ability to withstand fast rise-time, short duration EMP pulses. For example, a 30 joule rated varistor was destroyed with a 10^{-4} joule pulse from a simulated EMP source.[3] A 50 watt steady state rated zener diode can burn ou. with a pulse of 10^{-2} joules and a 10 watt steady state rated zener diode can burn out with a pulse of $5x10^{-3}$ joules.

For purposes of establishing a frame of reference, lightning has been compared with EMP, largely because of the historical information gathered in the study of meteoric electricity and its



Normalized Power Spectrum of EMP
Figure 1

effects on electronic equipment. Although lightning strokes are fast, 5 to 10 microseconds to crest, the transient voltage pulses induced into cables struck by a lightning discharge are stretched up to an order of magnitude or more. This transformation occurs because of the line inductance, end (termination) capacity, and the fact that lightning has a definite source of feed point. However, it is doubtful whether currents from distributive sources, such as EMP (or far-field lightning), would be stretched when conducted along cables.[4] Because of this difference, along with the high frequency energy present in an EMP, entirely new techniques must be considered when protecting against EMP exposure.

EFFECT OF CIRCUIT INDUCTANCE

Because of the fast rise-times of EMP, of the order of 5,000V/nanosecond and faster, inductive effects which generate voltage spikes described by the relationship

$$V = L\frac{di}{dt}$$

can be very significant. That which may appear to be negligible inductance, can be the source of voltage surges which can destroy sensitive components. Excessive lead lengths in transient suppression devices may very well be the source of destructive effects from which the device was inserted to give protection! The magnitude of "overshoot" voltage, or pulse energy leakage, due to length of device interconnecting leads is graphically illustrated in the following controlled series of tests.

TransZorbTM* silicon transient voltage suppressors were used in these experiments because of their fast "sub-nanosecond" response characteristics. The oscillogram in Figure 2 shows the open circuit voltage 5kV test pulse impressed upon the devices in subsequent surge tests and the oscillogram in Figure 3 depicts the 100A current pulse for the device under test. Because of the extremely low impedance of the suppressor under avalanche conditions, of the order of 50 milliohms, all devices in subsequent tests yielded approximately the same readout, approximately 100A, for current through the device. Suppressors of the 30V type, with varying lead lengths, were used to illustrate the effects of inductance in a transient suppression circuit.

Figure 4 depicts the overshoot (pulse) voltage produced under a 5kV pulse by a 30V silicon avalanche transient suppressor having 3 inch leads on each end. The magnitude of the voltage spike generated by the inductance in the leads is about 1200V peak and 20 nanoseconds in length.

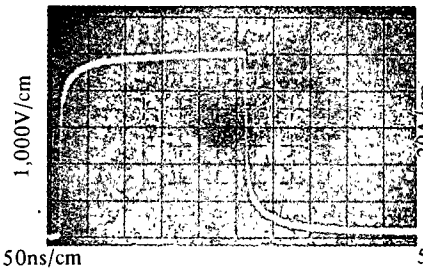


Figure 2–Voltage Test Pulse

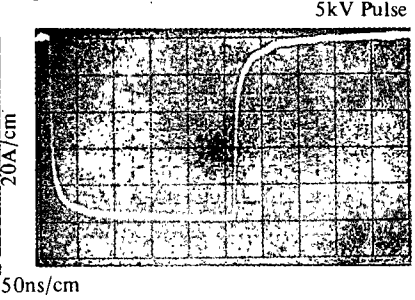


Figure 3–Current Pulse Under Test Load

The energy of this pulse produced in the protective circuit using the relationship

$$E = \int P\,dt$$

is calculated to be $1.5x10^{-4}$ joules. An EMP pulse of this magnitude will burn out FETs and some types of switching transistors.

The next oscillogram (Figure 5) shows the overshoot of the same device also under a 5kV pulse except with 1¼ inch leads at each end. Reduction in lead length brings about a reduction in the inductive voltage spike. The voltage overshoot for this device is about 800V with a pulse width of 10 nanoseconds. Energy produced by this pulse is calculated to be $7x10^{-5}$ joules. EMP pulses of this magnitude will burn out FETs, microwave diodes and germanium diodes.

In Figure 6, the same device is shown except it is terminated at the package and is virtually leadless externally.

When the external lead lengths are reduced to zero, there is yet a measurable overshoot voltage contributed by inductance of the lead wires within the package itself. The energy produced by this inductance under a 5kV pulse is calculated to be $6.7x10^{-7}$ joules. This is sufficient to cause burn-out of microwave diodes.

By modifying the device package into a disc and removing virtually all of the inductance from within the package and simultaneously reducing inductance of the insertion method, the inductive overshoot is reduced even farther as shown in Figure 7.

The amount of energy leakage with a 5kV pulse is unresolvable from the oscillogram made with the same vertical sensitivity as for the previous tests. Figure 8 depicts the same device and conditions as Figure 7 except the vertical sensitivity has been reduced from 200V/cm to 10V/cm.

Energy leakage through this system above the clamping voltage is calculated to be $1.5x10^{-9}$ joules. This is below the threshold of destruction for semiconductor devices.

INSTRUMENTATION AND TESTING

The instrumentation shown in Figure 9 was used to generate simulated EMP pulses and to record the effects of those pulses on devices in the previous tests. The power supply delivers a square wave pulse of 250 nanoseconds duration (Figure 2) with a rise-time of 5kV/nanosecond from a 50 ohm source. All devices in these tests were surged with 5kV pulses.

It is interesting to note that power dissipation in the TPD is not all absorbed on the first pulse. Multiple reflections occur which bounce back and forth between the entrance end of the coaxial cable and the suppressor. Figure 10 depicts the damped current pulses under simulated conditions of 10kV EMP pulse.

*TransZorb–Trademark of General Semiconductor Industries, Inc.

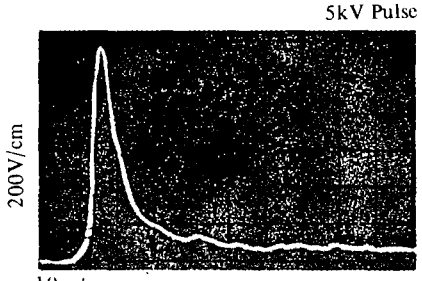


Figure 4

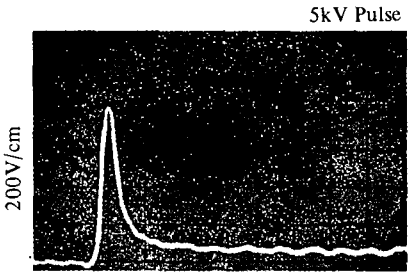


Figure 5

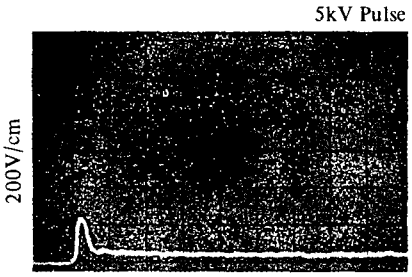
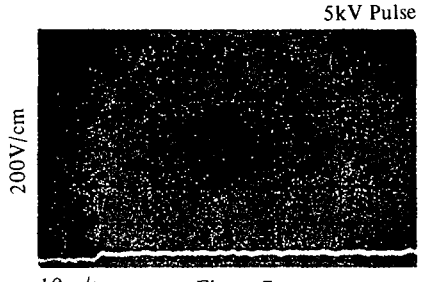


Figure 6



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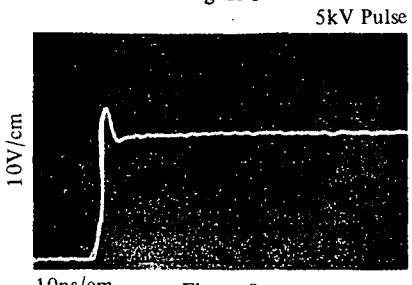
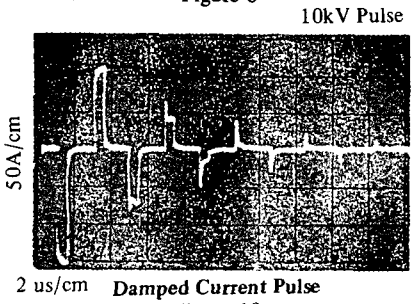
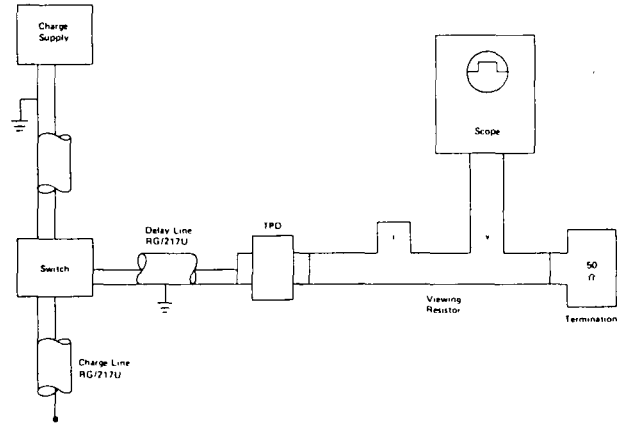


Figure 8



Damped Current Pulse
Figure 10



Pulse Generating and Measuring Equipment
Figure 9

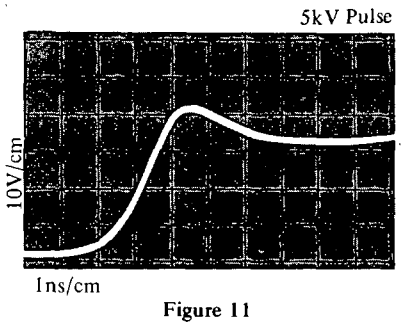
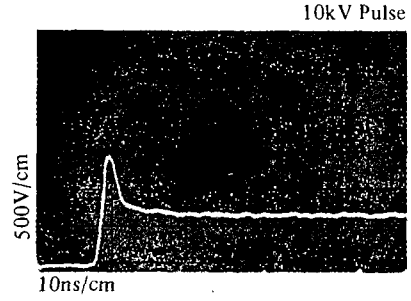
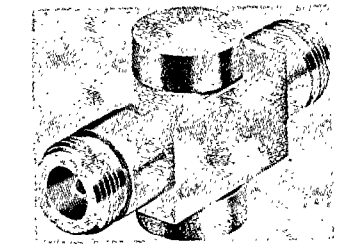


Figure 11



Missile System TPD Response Characteristics
Figure 12


Low Inductance TPD
Figure 13

EMP SUPPRESSION USING TRANSZORBS

Early studies performed under the direction of the U.S. Army Mobility Equipment Research and Development Center proved the feasibility of using silicon avalanche devices for EMP suppression.[5] This work incorporated the use of standard TransZorb product in the 1.5K6.8A through 1.5K200A series which are relatively new transient protectors on the market. These devices are characterized by small size and high transient power handling capability which is 1,500 watts for 1 millisecond up to 100,000 watts for 100 nanoseconds. Protection voltages available range from 5V through 200V for the standard product. Devices can be stacked in series to yield higher voltages as required. For higher power dissipation, devices can also be stacked in series or parallel depending on the design required.

Clamping of EMP is achieved through avalanche breakdown, a phenomenon which occurs when the device voltage is exceeded. Unlike SCRs and gas gaps, the voltage does not drop to a small fraction of the "striking" voltage upon initiating current flow. Hence, there is no need for a series voltage dropping resistor in dc circuits. The solid state avalanche phenomenon is fast. Figure 11 depicts a TransZorb (solid state avalanche device) protecting against a simulated EMP pulse of 5kV from the test setup as shown in Figure 9. The horizontal sweep has been resolved to 1 nanosecond per centimeter. It can be seen from this oscillogram that the clamping action is indeed rapid, in the one nanosecond range. The energy leakage of the pulse past this protective device is of the order of 10^{-9} joules, far below the threshold of damage to semiconductor devices.

COPING WITH CAPACITANCE

Large area silicon pn junctions of the type used in the TransZorb inherently posses high electrical capacitance. A graph showing capacitance vs breakdown voltage for this device is shown in Figure 14.

For DC and low frequency applications, these values of capacitance are satisfactory; however, for high frequency applications such as receiver front-ends and fast switching logic, the high capacitance loads the circuit to the extent that the signal is attenuated beyond an acceptable level. Methods of effectively reducing the capacitance are shown in Figure 15. These circuits illustrate insertion of a low capacitance diode in series with a TransZorb to attain a suitable low capacitance value as required by the system being protected.

General requirements for the low capacitance diode are:

(1) the surge handling characteristics in the direction of forward bias must be compatible with protection requirements;
(2) the reverse breakdown must be higher than the TransZorb maximum clamping voltage; and
(3) the device must be fabricated using "P" type silicon for minimum overshoot for fast rise time transients.

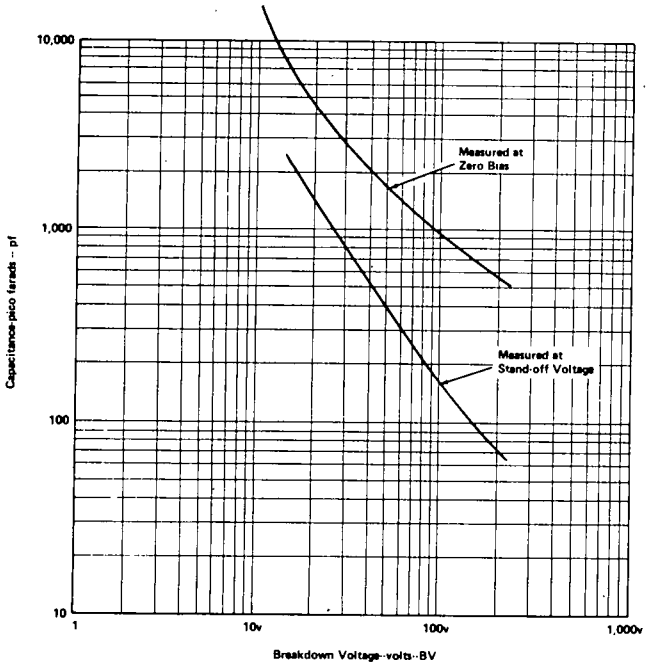


Figure 14
Typical Capacitance vs Breakdown Voltage for 1.5kw TransZorb

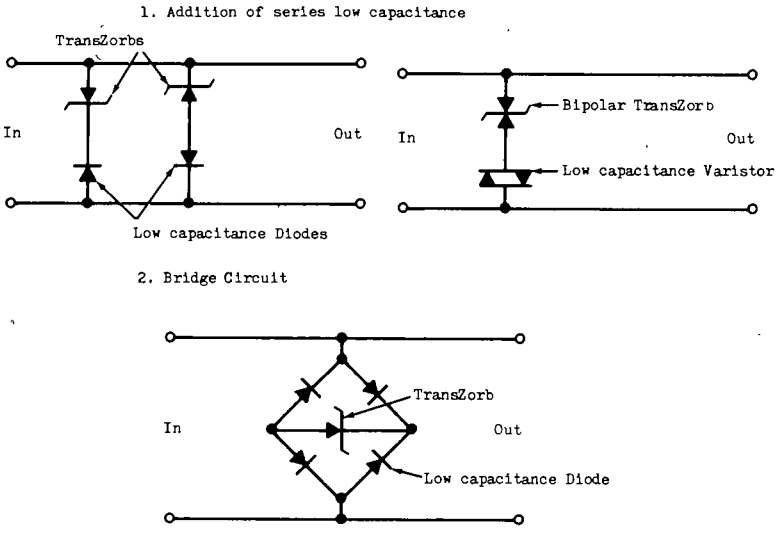


Figure 15:
Methods of Reducing Capacitance in Low Voltage Devices

EMP DAMPED SINUSOIDAL WAVE

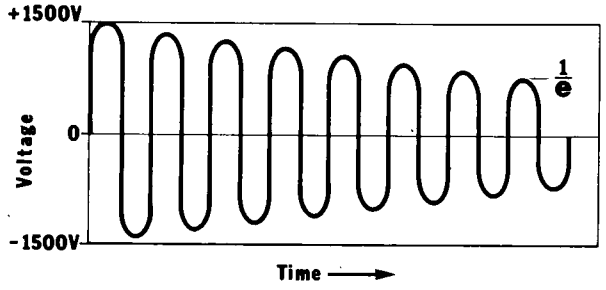
Damped sinusoidal pulses are produced when primary induced EMP currents, such as those in the skin of a hardened enclosure, are subsequently induced into cables on the enterior of the container. The mathematical description of the voltage component of the pulse is described below as:

$$V_{(t)} = 1500e^{-\frac{\pi f_0 t}{Q}} 2 \text{ SIN } (2\pi f_0 t)$$

Where: $Q \geq 24$

f_0 = 10kHz through 100MHz

The wave form is as shown in Figure 16 with eight cycles for the pulse to decay to $\frac{1}{e}$ (7).



EMP Damped Sinusoidal Pulse
Figure 16

From the information given in Table I, it would seem that the TransZorb is certainly qualified for the role of secondary induced EMP protection. They might even appear to be substantially over-rated; however, there are normal aircraft transients generated whenever motors, solenoids, or other inductive loads are de-energized.

One of the most extensive studies on aircraft transients was performed by the Boeing Company on the KC 135 aircraft. Their report No. T6-2408 describes aircraft transient voltages measured at 25 different locations in the electrical system with peak voltages up to 800V having typical durations of 0.32 milliseconds.

Because of the "normal" transients which do exist in aircraft electrical systems, it behooves the engineer to consider both internal and external sources when specifying protection devices.

EMP Damped Sinusoidal Wave			Transzorb Protection Capability			
frequency	$\frac{1}{e}$ decay time	pulse amplitude	5V (1N5907)	33V (1N5645A)	91V (1N5656A)	200V (1N5665A)
10 kHz	0.8msec	1A	380A	88A	32A	14.5A
800 kHz	10 μsec	10A	2860A	660A	240A	110A
2 MHz	4 μsec	10A	6290A	1430A	520A	238A
100 MHz	80nsec	3A	12800A	2970A	1800A	495A

Table I TransZorb Protection Capability

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