Printed Circuit Board Suppression Concepts for EMC Compliance

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PART 2

THIS IS THE SECOND of a two-part article that presents fundamental EMC concepts related to designing suppression for EMC compliance into printed circuit boards (PCBs). Part 1 appeared in ITEM 1998. Together, these two articles create one comprehensive document. Both articles present explanations of EMI and various design and layout techniques that are easily implemented. These techniques provide the reader with a fundamental understanding of how one can implement RF suppression during layout which will minimize EMI threats at the beginning of a design project. Topics examined in Part 1 included how and why EMI exists, image planes and stackup assignments, and bypassing and decoupling.

Routing Clock Traces

To a significant degree, oscillators, associated components, and clock traces account for most of the emissions generated within a PCB. A clock circuit area is defined as the functional area that physically contains the oscillator, buffers, drivers and associated components, both active and passive. RF emissions are the result of both the rise and fall time (edges rate) as well as the fundamental clock frequency of digital components switching between logic states.

To determine the spectral distribution of RF energy that will be developed, use Equation 1. This equation does not take into account harmonics created from the primary frequency. A product design must take into consideration up to the tenth harmonic of the highest internally-generated frequency created within the PCB.

$$f_{max} = \frac{1}{\pi \cdot t_r} \qquad (1)$$

where

f_{max} = Maximum generated RF frequency range

t_r = Edge rate (rise or fall time—use the faster of the two)

For example, a 2-ns edge rate, typical of common clock drivers and components, can be expected to radiate significant RF energy up to 160 MHz, falling off rapidly above that frequency. The possible significant RF spectrum is 10 • f_{max} or 1.6 GHz, which includes the harmonic content of the main frequency component.

To minimize emissions that may be created within a PCB, traces rich in RF energy should always be *manually* routed. After successful routing of these high threat traces, we may automatically route the remaining nets.

COMPONENT PLACEMENT

RF generating components should be located in an area of the PCB as close to, or adjacent to, a ground stitch location (to chassis ground if multipoint grounding is used), rather than along the perimeter or near the I/O section. If a trace with RF energy travels to a daughter card, ribbon cable, interconnect or the like, this clock circuit must be located some distance from this interconnect, but not so far away as to make the interconnect trace electrically long, which could cause a signal integrity problem.

For these single-ended traces, the clock trace must be terminated directly at the interconnect to prevent an open-ended transmission line. It is imperative that this be comprised of a single point-to-point connection. Termination of clock traces at interconnects guarantees signal quality when the connector is not provided. In addition, trace termination prevents excessive RF currents from coupling into other areas susceptible to RF corruption. Devices that create clock signals (oscillators, clock drivers, buffers and the like) must be installed directly on the PCB—do not use sockets! Sockets add lead length inductance to the trace (LdI/dt). Lead length inductance allows ground noise voltage to develop by creating a difference in reference voltage between two points. In turn, ground noise voltage generates common-mode RF currents, which will radiate or couple into susceptible areas.

TRACE LENGTHS

During layout, components that use clocks or periodic signals should be located such that the traces are routed for the shortest distance possible (minimal Manhattan length) with a

minimal number of vias. Ground vias may, however, be required. These are discussed later. Vias add inductance to a trace (approximately 1-3 nH each). Inductance in a trace may cause functional signal quality concerns and potential RF emissions, as presented earlier. This trace inductance is added to the sum of the inductance of all vias and the bond wires internal to a component's package. The faster the edge rate of a clock signal, the more this design rule approaches mandatory status. If a periodic signal or clock trace must traverse from one routing plane to another (layer jump), this transition should occur only at a component lead at 0-V reference or ground, and not anywhere else. This is discussed later in the section on layer jumping (or use of ground vias). The goal is a maximum of two vias per route, one at the source, and one at the load, if a stripline configuration is provided.

The old directive to "keep clock lines short" will always be valid. The longer the trace, the greater the probability that RF currents will be produced, and a larger spectral distribution of RF energy created. Clock traces must be terminated to reduce ringing and creation of avoidable RF currents. This is because unterminated lines allow signal reflections to exist, which can also cause EMI to be created. Improperly terminated clock signals might also degrade the signal to the point of being nonfunctional.

DETERMINING ELECTRICALLY LONG TRACE LENGTHS

How do we determine if a trace is electrically long during component placement? A simple method exists that allows PCB designers to ascertain whether a trace requires termination or special treatment by the design engineer. The velocity of propagation within a trace is typically 60 percent the speed of light (based on the dielectric constant of the material used). The maximum permissible unterminated line length is calculated per Equation 2. This equation is valid when the two-way propa-

gation delay (source-load-source) is greater than, or equal to, the signal rise or fall time from a source driver.

$$L_{max} = \frac{t_r}{2 \, t'_{pd}} \qquad (2)$$

where

t_r = Edge rate of the transition (ns)
t'_{pd} = Propagation delay of 1" of line
L_{max} = Maximum round trip distance of the routed trace (centimeters)

When dealing with transmission lines, a PCB designer needs a quick rule-of-thumb during component placement that enables determination of whether a trace routed on a PCB is considered to be an electrically long trace. A simple calculation is available that approximates the length of a trace, to determine if it is electrically long, with a high degree of accuracy. When determining if a trace is electrically long, we must think in the time domain.

Equation 2 can be simplified as follows. Substituting the propagation delay of FR-4 material with a dielectric constant of 4.6 (at 10 MHz) for both microstrip (1.72 ns/ft) and stripline (2.26 ns/ft), use two simple, basic equations to calculate the maximum electrical line length before ter-

mination is required. The equations take into account the conversion from feet to centimeters. If the round trip, routed trace length is greater than L_{max}, then both signal functionality and EMI concerns exist. Figure 1 illustrates this equation for quick reference.

L_{max} = 9 • tr (for microstrip topology, in cm.) (3)
L_{max} = 3.5 • tr (for microstrip topology, in in.)
L_{max} = 7 • tr (for stripline topology, in cm.) (4)
L_{max} = 2.75 • tr (for microstrip topology, in in.)

For example, if a signal transition is 2 ns, the maximum unterminated trace length when routed microstrip is:

$$L_{max} = 9 \cdot tr = 18 \text{ cm (7")}.$$

When this same trace is routed stripline, the maximum unterminated length of this 2-ns transition is:

$$L_{max} = 7 \cdot tr = 14 \text{ cm (5.5")}.$$

If a trace is longer than L_{max}, termination should be implemented, as signal reflections (ringing) will occur in this electrically long trace. Ringing created by an impedance mismatch
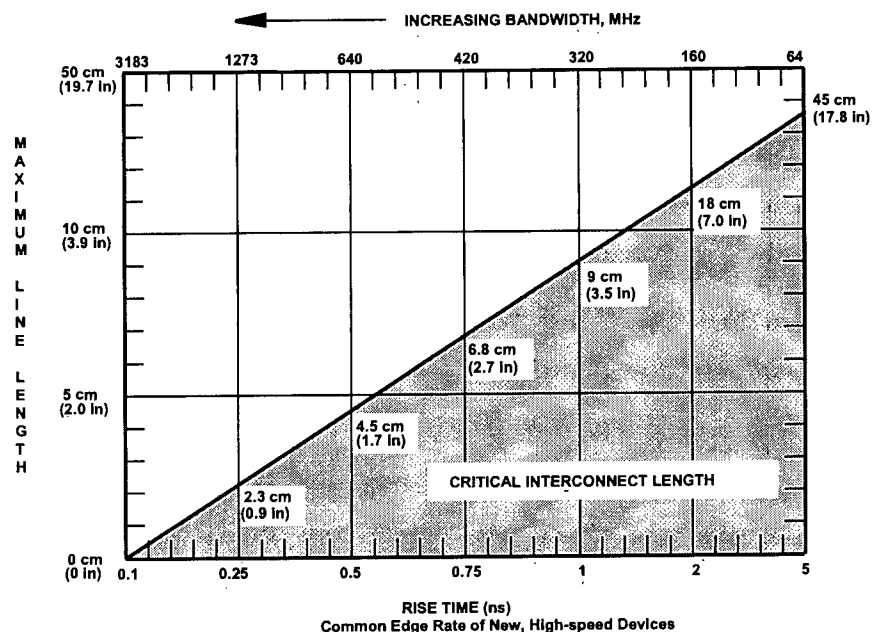

Figure 1. Maximum Unterminated Line Length Vs. Signal Edge Rate (FR-4 Material).

in an electrically long trace may also make the circuit non-functional, and could create RF currents within the trace (common-mode). Even with good termination, a finite amount of RF current will still be present within the trace.

For every signal, a time domain reflection occurs. There will always be a finite time period for a signal to travel from source to load, and then return from the load to source. An electrically long trace is a trace that allows the one-way (source to load) propagation delay to exceed ½ the clock cycle. If a second clock signal (edge transition) occurs before the reflection of the original reflected signal returns to the source, ringing will develop. Depending on the phasing of the reflection, overshoot or undershoot may occur, which will cause significant signal quality issues to be present. Signal degradation is a concern if the edge time of the signal constitutes a significant percentage of the propagation time between the device load intervals.

ROUTING LAYERS

A frequent concern is how to determine on which layer or planes clocks or periodic signals are to be routed. Clocks and periodic signals must be routed adjacent to a solid reference plane, preferably at ground or 0-V potential, not floating. This is true for both routing layers, x axis and y axis, also identified as the horizontal or vertical routing planes. Several issues must be remembered when selecting routing layers. These issues include which layers to use for trace routing, jumping between designated layers and maintaining a constant trace impedance throughout the trace route.

Figure 2 illustrates how to optimally route clock traces on different layers, assuming a multilayer stackup.

• A solid reference (image) plane must be used adjacent to the signal trace. Minimize routed trace lengths while maintaining a constant trace impedance (constant trace width). If series termination is used, connect the resistor directly

to the output pin of the component. After the resistor, place the via internal to the stripline layers.

• Do not route clock or sensitive traces microstrip if a six or more layer stackup is provided. The outer layers of the PCB should be reserved for large signal buses and I/O circuitry that does not create RF energy. When routing traces between layers, there may develop a change in the characteristic impedance of the trace (trace to reference plane), thus affecting performance and possible signal degradation.

If a constant trace impedance is maintained, and the use of vias is minimized or eliminated, the trace will not radiate any more than a coax.

LAYER JUMPING (USE OF GROUND VIAS)

When routing clocks or high-threat signals, we generally via the trace down to a routing plane (e.g., x axis) and then via this same trace to another plane (e.g., y axis) from source to load. This is shown in the poor routing method of Figure 2. It is generally assumed that if each and every trace is routed adjacent to an image plane, there will be tight RF coupling

between the signal trace and reference plane (flux cancellation). In reality, this assumption is incorrect.

When a jump is made from a horizontal to a vertical routing layer, the RF return current cannot make this jump. The return current must now find an alternate, low impedance path to complete the closed loop boundary requirements. This alternate return path usually does not exist when jumping a trace between layers. To minimize creation of EMI and crosstalk due to layer jumping, the following design techniques have been found to be effective.

• Route all clock and high-threat signal traces on only one routing layer.

• Verify that a solid 0-V reference, or ground plane, is adjacent to the routing layer with no discontinuities in the route, e.g., plane cuts or moats.

• If a via must be used for routing a sensitive (high-threat or clock) signal trace between the horizontal and vertical routing layer, incorporate corresponding ground vias at each and every via location where the axis jumps occurs.

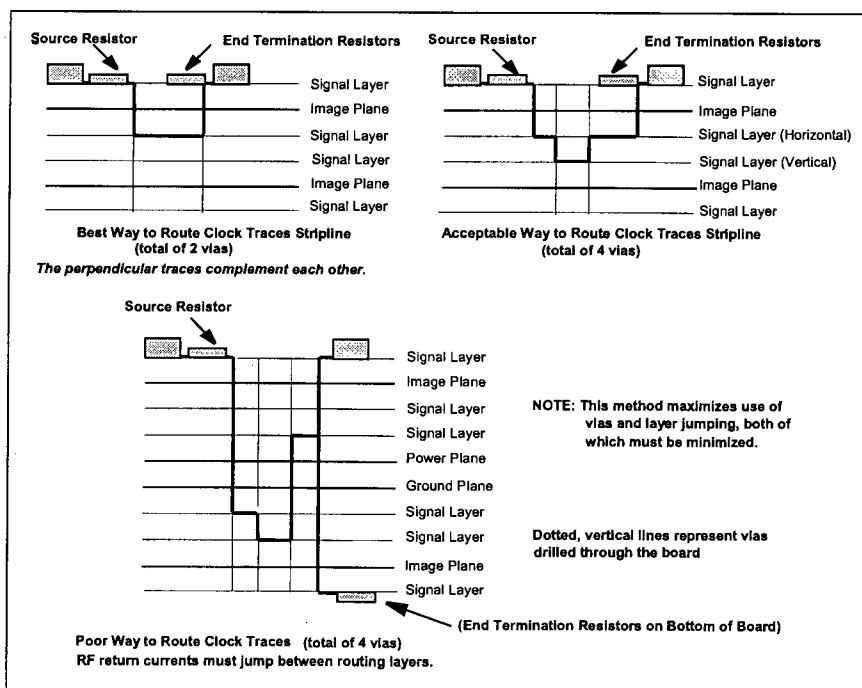A ground via is a via that is placed directly adjacent to each signal route

Figure 2. *Routing Clock Traces.*

via. Ground vias can only be used when there are multiple ground planes in the PCB. This via must connect all the ground planes together. Ground vias allow for a constant RF image plane return path to be present adjacent to a signal route, and provide a mechanism for optimal flux cancellation. The ground pin of a component (pin escape or breakout) makes an excellent ground via.

Impedance Control and Trace Termination

Trace termination assists in the reduction of RF energy in addition to insuring signal functionality and quality for performance reasons. In order to achieve optimal termination, the impedance (Z) of the trace or transmission line must be maintained within a certain percentage of its desired value. Typically, a trace will have an impedance between 45 and 120 ohms depending on how the PCB is constructed. In this section, we examine several methods of controlling the impedance of a trace within a PCB and discuss commonly-used termination methods for various applications.

IMPEDANCE CONTROL

With today's high technology products and faster logic devices, transmission line effects become a limiting factor for proper circuit operation. A trace routed adjacent to a reference plane forms a simple transmission line. A trace does not contain voltage, current or electrons. A trace transfers an electromagnetic field from source to load. To guarantee that the electromagnetic field does not incur a loss during transmission, or to allow signal reflections to be created, both the source and load impedance must be matched (maximum power transfer theorem). The major parameters describing transmission line impedance is trace width, distance spacing between the trace and reference plane and dielectric constant of the PCB material.

IMPEDANCE CALCULATIONS

The popular formulas used for microstrip and stripline were first published in the Motorola MECL System Design Handbook HB 205. Motorola popularized this formula set in the 1970's in conjunction with its ECL logic family. When these equations were published, the impedance was assumed to be in excess of 75 ohms, with traces 0.020-inch thick and a height separation of 0.020-inch between trace and reference plane. As a result, these commonly-published formulas achieve accuracy within a tolerable range for a majority of product designs.

Today's products, however, are commonly fabricated at 0.005 inches or less. With such close trace-to-plane separation, effects of the reference plane related to the trace become pronounced. These equations fail to provide accurate answers when low-impedance clock distribution traces are provided (i.e., 20 ohms).

We must maintain trace impedance at a constant value throughout the entire route. Depending on application, impedance tolerance levels may differ by +/-10%. Vias within a trace route, (at approximately 1-3 nH inductance and 2-pF capacitance each) may cause the overall impedance of the trace to change from a desired value by the equation $Z = \sqrt{L/C}$. For critical signals, an impedance discontinuity in the transmission path may cause functionality concerns (time domain). In addition, vias prevent RF return currents from finding a low impedance return path back to their source whenever a trace changes a routing layer (layer jumping). Layer jumping is a primary cause of EMI, as a continuous return path for RF return currents will not be present.

When developing a stackup assignment, determine the trace impedance desired prior to routing any trace. Selecting a proper trace width is necessary to maintain a constant impedance throughout the trace route. For example, for a symmetrically-balanced 6-layer PCB, 0.010-inch trace width, and dielectric constant $\epsilon r = 4.3$,

we have 66-ohm impedance for embedded microstrip and a 97-ohm trace for outer microstrip. Using this example, if traces are jumped between routing layers with different impedances, a standing wave ratio (SWR) of 1:1.5 occurs. If the length of the trace is significant, functionality concerns become dominant, not EMI.

When a trace jumps layers, such as stripline to microstrip, with a 1:1.5 mismatch, a simple design technique to maintain constant impedance is to change the routed trace width on different layers. For the example above, the outer microstrip trace should be 32 mils (0.032") wide while the embedded microstrip trace is 12 mils (0.012") wide for a constant 55 ohm transmission line. Although easy to implement, changing the width of selected traces on a routing layer is a design concept that is usually not implemented for various reasons. This is because a PCB designer, or the layout specification requirement, mandates all traces within the PCB to be the same width for consistency, especially if an autorouter is used. In addition, less room exists for routing many traces' outer microstrip if wide trace widths exist. The concept of maintaining the same trace width for all traces in new, high-speed, high-technology designs is now an outdated concept.

TRACE TERMINATION

It is common practice to daisy chain periodic signal and clock traces for ease of routing. Unless the routed distance is small between loads, (with respect to the propagational delay of the routed trace), signal reflections may occur. Daisy-chaining affects signal quality sometimes to the point of non-functionality. Therefore, *radial* connections for fast edge signals and clocks are preferred. Examples of these two routing methodologies are shown in Figure 3.

If a clock trace must be electrically long, and it contains edge transitions faster then 2 ns, the trace should be routed as a transmission line. Use of a transmission line structure mini-

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Poor Trace Routing for Clock Signals
(Note Daisy Chaining of Clock Signal)

Optimal Trace Routing for Clock Signals
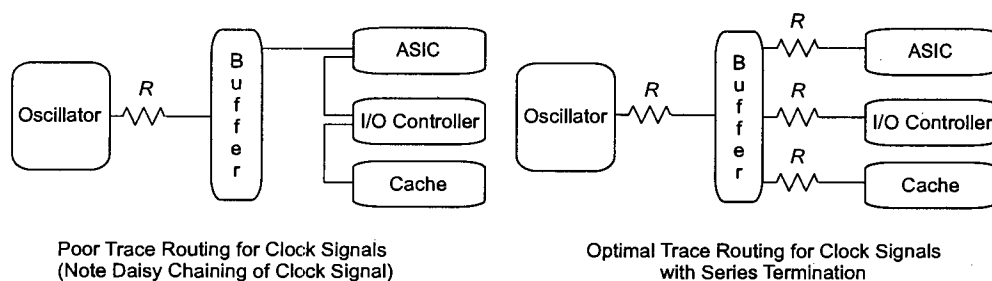with Series Termination

Figure 3. Termination of Clock Traces.

mizes ringing and reflections (signal integrity concerns). In addition, we maintain a constant impedance for the trace. Ideally, trace impedance should be kept at 10% of nominal value. In some cases, 20% to 30% is acceptable only after careful consideration is made as to whether signal integrity will be affected by this larger tolerance level.

To assure optimal signal quality, trace termination may be required. There are five termination methods commonly used. These methods are dependent on the complexities of the layout geometry, component count, power consumption and other items detailed below. When a source driver is overloaded, termination can degrade the transmitted signal if incorrectly specified or implemented.

Five commonly-used termination methods are listed below and detailed in Figure 4.

1. Series termination resistor
2. Parallel termination resistor
3. Thevenin network
4. RC network
5. Diode network

SERIES TERMINATION RESISTOR

Series termination is optimal with a single source driver and single load. Use the series resistor when the output impedance of the driver, ($Z_{\text{output driver}}$) is less than the loaded characteristic impedance of the trace (Z_{trace}). In other words, $R_s = Z_{\text{trace}} - Z_{\text{output driver}}$. Locate the resistor directly at the output of the driver without the use of a via between the two, if at all possible.

- When the output impedance ($Z_{\text{output driver}}$) plus series resistor (R_s) equals the characteristic impedance of the trace (Z_{trace}), the voltage waveform at the output of the resistor is divided evenly with half of the voltage transmitted to the receiver. If the receiver has a very high input impedance, the full waveform will be observed immediately, while the source will receive the reflected waveform at 2 • tpd (round trip propagation delay). Since devices have different input and output impedances, especially the source driver, use of a series resistor may not be optimal.

PARALLEL TERMINATION RESISTOR

For parallel termination, a single resistor is provided at the end of the trace route. This resistor, *R*, must have a

value equal to the impedance of the trace or transmission line. The other end of the resistor is tied to a reference source, usually a ground. Parallel termination may add a small propagation delay to the signal due to a combination of both resistance and distributed capacitance within the transmission line structure.

A disadvantage of parallel termination is consumption of DC power, since the resistor is generally in the range of 50 ohms to 150 ohms. The driver must source current when driving the trace logic high. In applications where power consumption is critical, e.g., battery-powered products (notebook computers, for example), parallel termination is a poor choice. An increase in drive current will cause an increase in power consumption from the power supply, an undesirable feature in battery-operated units.

THEVENIN NETWORK

Thevenin termination has one advantage over parallel termination. One resistor is connected to the power rail, the other resistor to ground. Unlike parallel, Thevenin allows for optimizing the voltage transition point between logic HI and logic LOW. When using a Thevenin network, consideration in choosing the resistor values must be made to avoid improper setting of the voltage reference level for both logic HI and LOW. The ratio of R1/R2 also determines the relative proportions of logic HI and LOW drive current. The Thevenin equivalent resistance must be equal to the characteristic impedance of the trace. Like parallel termination, Thevenin consumes power as the source driver must either sink or source current on the trace at all times.
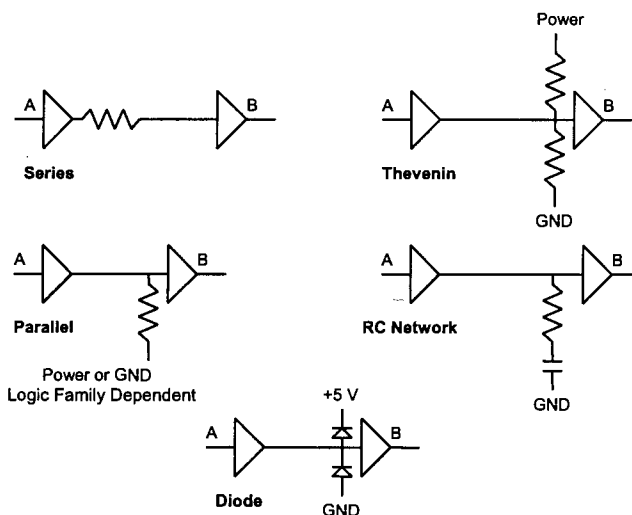

Figure 4. Termination Methodologies.

RC NETWORK

The RC network (also known as AC) works well in both TTL and CMOS systems. The resistor matches the characteristic impedance of the trace (identical to parallel). The capacitor holds the DC voltage level of the signal. The source driver does not have to provide drive current to the terminating network. As a result, AC current (RF energy) flows to ground during a switching state. The capacitor allows RF energy (which is an AC sine wave component, not the DC logic level of the signal), to pass through to a 0-V reference. Although an additional propagation delay is presented to the signal due to the RC time constant, less power dissipation exists over parallel or Thevenin termination. From the viewpoint of the circuit, all three end termination methods are identical. The main difference lies in power dissipation, with RC consuming far less power than the other two.

The termination resistor must equal the Zo of the trace while the capacitor is generally very small (20-600 pF). The RC time constant must be greater than twice the loaded propagation delay (round trip travel time). RC termination finds excellent use in buses containing similar layouts.

DIODE NETWORK

The diode termination method is commonly used for differential or paired networks and analog devices. Diodes are used to limit overshoot and undershoot while providing low-power dissipation. The major disadvantage of diodes lies in their frequency response to high-speed signals. Although overshoots and undershoots are prevented at the receiver's input, reflections will still exist, as diodes do not affect trace impedance or enhance signal functionality. To gain the benefits of both techniques, diodes may be used in conjunction with the other methods discussed herein to minimize reflection problems.

Miscellaneous Suppression Techniques

There is more than one way to design and layout a PCB. All techniques presented here have a proven track record for preventing the creation of RF energy, reducing common-mode currents created from component switching logic states, and preventing ground loops in the RF return path from occurring.

Items presented include the 20-H rule, the 3-W rule, moating and isolation, and grounded heat sinks.

20-H RULE

Between the edges of the power and ground planes in a multilayer PCB, magnetic lines of flux link the two planes. This interplane coupling is called fringing and is generally observed on only very high speed PCBs. When using high-speed logic and clock circuits, the power and ground planes can couple these flux lines to each other, thus radiating RF energy into free space. To minimize this coupling effect, the power planes must

be physically smaller than the closest reference ground plane per the 20-H rule. Figure 5 shows the effects of RF fringing from the edges of a PCB.

To implement the 20-H Rule, calculate the physical spacing (distance) between the power plane and its nearest ground plane. This distance includes the thickness of the core or prepreg material. If a distance separation of 0.006 inches is assumed to exist between the two planes, calculate "H" as (20 • 0.006 inches) = 0.120 inches. Physically make the power plane 0.120 inches smaller than the ground plane on all four sides if the straight line distance along the edge of the PCB exceeds $\lambda/20$ of the higher generated frequency within the PCB. If a power pin to a component is located within this isolated area (absence of copper), the power plane may be jogged to provide power to this isolated pin. This is detailed in Figure 6. What we are concerned with is the linear straight-line distance along the edge between the planes. Any linear length between the parallel plates acts as a resonant antenna based upon the physical length of the driven elements relative to the fre-
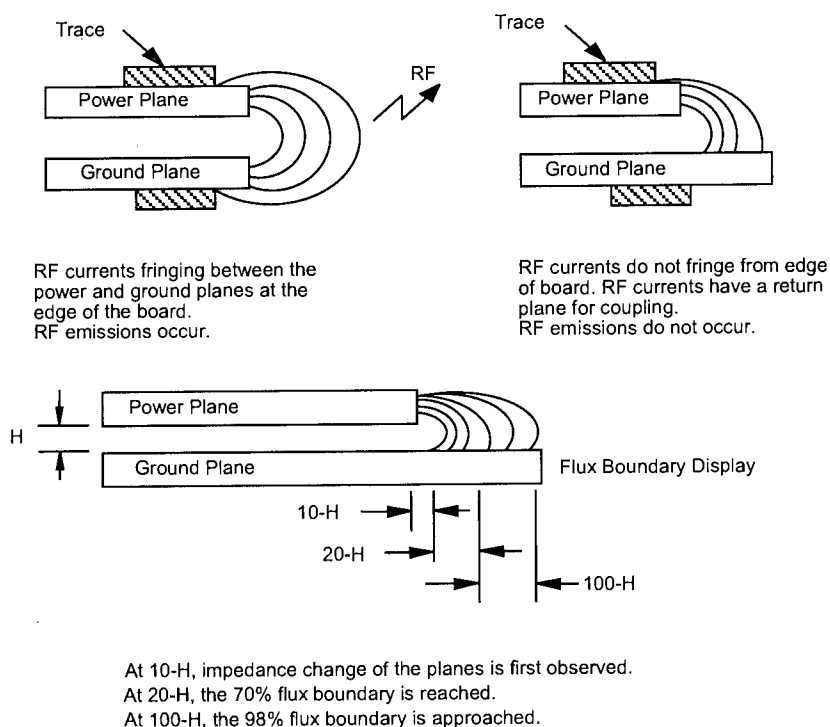

Trace

Power Plane

Ground Plane

RF currents fringing between the power and ground planes at the edge of the board.
RF emissions occur.

Trace

Power Plane

Ground Plane

RF

RF currents do not fringe from edge of board. RF currents have a return plane for coupling.
RF emissions do not occur.

H

Power Plane

Ground Plane

Flux Boundary Display

10-H

20-H

100-H

At 10-H, impedance change of the planes is first observed.
At 20-H, the 70% flux boundary is reached.
At 100-H, the 98% flux boundary is approached.
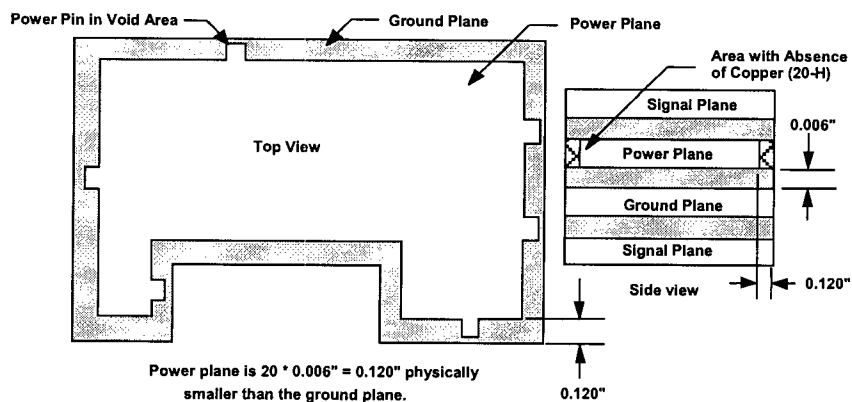
Figure 5. *Concept of the 20-H Rule.*

Figure 6. *Implementing the 20-H Rule.*

quency of RF energy that exists within the power and ground planes.

When using the 20-H Rule, signal traces routed adjacent to the power plane must be rerouted inward to be physically adjacent to the solid reference (power) plane, not over the absence of copper area. There can be no exceptions. It becomes important for the PCB designer to examine all planes individually for proper implementation and to verify 20-H of the power plane and to guarantee that traces are physically adjacent to a solid RF return path or plane.

3-W RULE

Use of the 3-W rule is required to minimize coupling between traces rich in RF energy. The 3-W rule states that "the separation distance between traces must be three times the width between traces measured from centerline to centerline." Otherwise stated, "the separation distance between two traces must be greater than two times the width of a single trace." For example, a trace is 0.006 inches wide. No other trace can be physically located within 0.012 inches of this trace, edge-to-edge. As observed, much real estate is lost in areas where trace isolation occurs. An example of the 3-W rule is shown in Figure 7.

The advantage of using the 3-W Rule is that it assists in the reduction or elimination of crosstalk between signal traces. Crosstalk occurs when RF flux created in one trace couples onto an adjacent trace. Details of the actual mechanism is beyond the scope

of this article. Design engineers generally simulate a PCB layout to determine if crosstalk exists. Use of 3-W can save the design engineer many hours of extensive simulation analysis if time does not permit for computer simulation. Clock traces and high threat signals are prime candidates for mandatory use of 3-W.
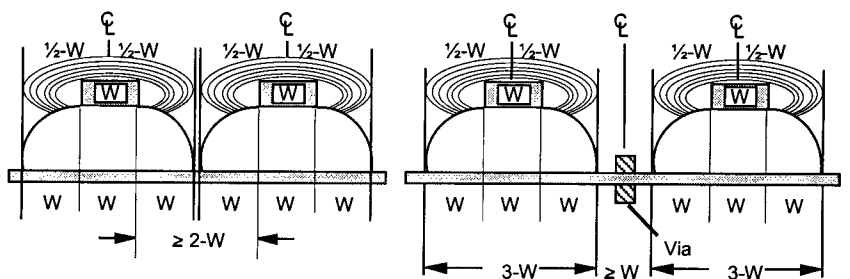
ISOLATION AND MOATING

Isolation refers to the physical separation between components, circuits and power planes from other devices, functional areas, and subsystems. Allowing RF energy to propagate to different parts of the PCB by radiated or conductive means will cause problems not only in terms of EMI, but also with regard to functionality.

Isolation is created by absence of

copper. Absence of copper is a wide separation (typically 25 mils minimum) within all solid planes of the PCB. In other words, an isolated area similar to an island in the middle of the board is created. Only those traces required for operation or interconnect can travel to or through this separated area.

The area characterized by absence of copper is also identified as a moat. A moat serves as a keep-out zone for signals and traces that are unrelated to the moated area's function or its interface. An example of a moat for an I/O connector is shown in Figure 8. It is common to implement moating in the middle of a PCB to separate a clock generation circuit from non-related components susceptible to RF corruption through common-impedance coupling of the power and ground planes. Moated areas include analog-to-digital partitions, I/O interconnects and similar applications.

The reason we implement partial moats in the middle of a board is to force RF return currents to travel a specific path to a chassis ground location through the path of least impedance. We control the flow of RF return current by forcing it to take a predetermined path to ground per our design requirements, not leaving this to chance. If a moated area is separated from other sections of the board,

The distance spacing between both traces must have a mimimum overlap of 2W.

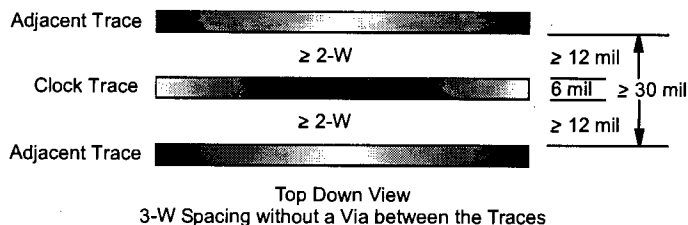For the via, add angular diameter which includes both the via and angular clearance.

Top Down View
3-W Spacing without a Via between the Traces

Figure 7. *Implementing the 3-W Rule.*

this isolated zone keeps its internally-generated RF ground noise to itself. Generally, moated areas are small enough to not cause RF currents to be created. We also want to prevent clock generation circuitry from coupling their RF currents into nearby I/O connectors and other circuits susceptible to RF corruption.

If we moat or isolate an area 100 percent, then how does one cross this moat with traces? Three methods exist:

- Route all traces across the moat on only one side of the circuit area to prevent RF return currents from creating a ground loop through two sides of the moat.
- Cross the moat with a ferrite bead-on-lead or common-mode choke.
- Route all traces through a bridge.

Bridging is shown in Figure 9. Note that all signals that travel from the main section to the I/O area pass through a bridge or opening in the moat. No trace must cross the moat under any condition! The RF current return path must be physically next to the routed signal trace to cancel out magnetic lines of flux that exist between the two. If a moat violation occurs, the RF return current must take a longer path home, which allows for the creation of undesired, common-mode RF current.

In addition to minimizing the RF return path, ground return currents can be easily directed into the ground reference system. A ground point must be located close to the bridge opening, so it can source RF currents to chassis ground if multipoint grounding is provided. Optimal sourcing of RF currents to a 0-V reference keeps ground plane noise from corrupting other functional areas, or I/O interconnects, by common-impedance coupling.
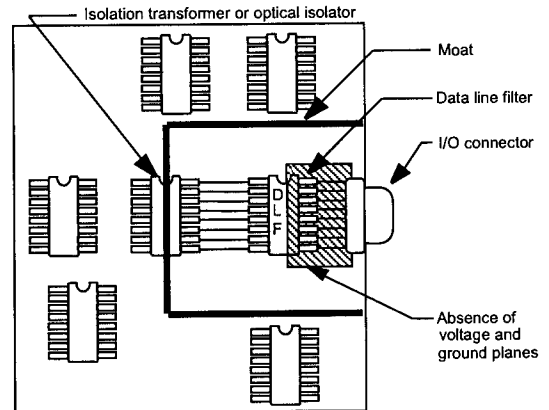
GROUNDED HEAT SINKS

Grounded heat sinks are a new concept in PCB suppression that finds use in specific applications and for certain components. Grounded heat sinks are sometimes required when using processors with internal clocks

in the 75 MHz range and above, or for components that create large amounts of common-mode currents internal to the device package. These devices require more extensive high-frequency decoupling and grounding than most other parts of a PCB.

RISC processors or VLSI components usually have a high internal self-resonant frequency. This high self-resonant frequency is a combination of the manufacturing process and internal clock speed. As a result, these components can radiate RF energy more so than most other components, even clock traces, if RF suppression techniques are not incorporated by the component manufacturer. Any attempt to remove this radiated RF energy, using standard suppression techniques, is nearly impossible, except through the use of a heat sink as a common-mode decoupling capacitor. The heat sink is used in addition to the standard differential-mode decoupling capacitors normally provided. A common-mode decoupling capacitor provides an AC shunt to remove common-mode energy within a device package, transfering this energy into a 0-V reference system.

The wafer (or die) internal to the component's assembly is generally located closer to the top of the device

Note - DLF refers to data line filter (or common-mode choke).

Figure 8. Moating and Isolation Concept.

package, rather than the bottom, where connection to the I/O pins occur. Height separation from the die to the heat sink is smaller than the height separation between the die and the nearest 0-V reference plane internal to the PCB. Common-mode RF currents generated internal to the package, have no place to couple; hence, RF common-mode currents radiate into free space. Differential-mode decoupling capacitors will not remove common-mode RF energy.

An electrical representation of a typical metal heat sink used for thermodynamic purposes is shown in Figure 10, while Figure 11 shows the implementation of a grounded heat sink design.

A grounded heat sink is always at a 0-V reference potential. The active component (the die within the device package) is at RF voltage po-
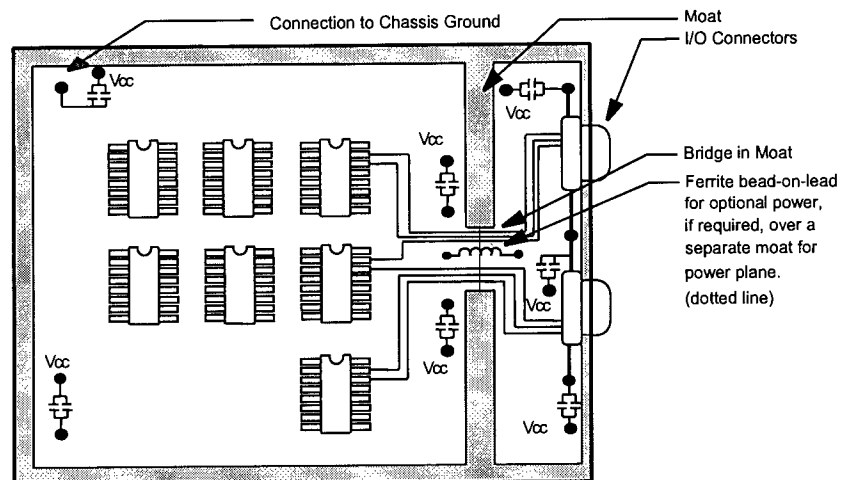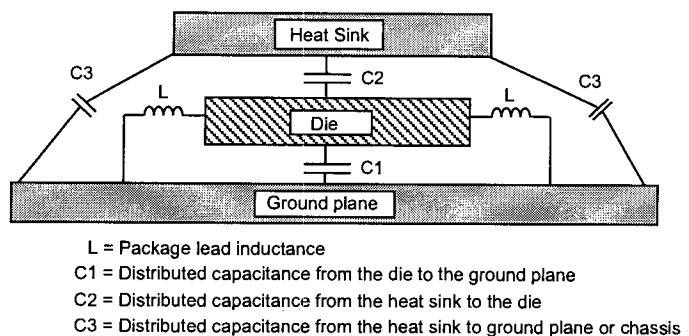

Figure 9. Proper Use of Bridging a Moat.

L = Package lead inductance
C1 = Distributed capacitance from the die to the ground plane
C2 = Distributed capacitance from the heat sink to the die
C3 = Distributed capacitance from the heat sink to ground plane or chassis

Typical self-resonant frequency of VLSI processors is approximately 400-800 MHz.

Figure 10. *Electrical Representation of a Metal Heat Sink.*
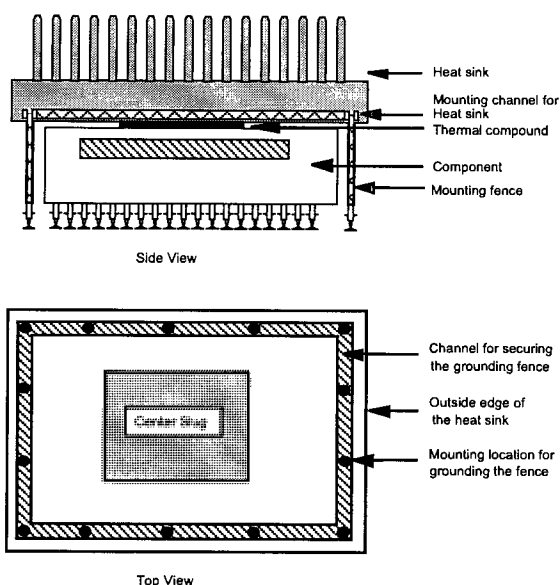

Side View

Top View

Figure 11. *Implementation of a Grounded Heat Sink.*

tential. The thermal compound between the package and the heat sink is a dielectric material. The definition of a capacitor now exists. Thus, a grounded heat sink works as one large common-mode decoupling capacitor. Discrete capacitors located on the top of the device package, and directly on the PCB, are always provided for differential-mode decoupling. This common-mode decoupling capacitor sinks RF common-mode currents generated *internal* to the processor and sends this current to ground. A common-mode decoupling capacitor will only work if its self-resonant frequency is above the highest frequency of RF energy to be suppressed. The difference between a differential-mode decoupling capacitor and a common-mode heat sink capacitor is that differential-mode capacitors are connected between a power and ground reference source. A common-mode capacitor connects to ground and AC couples RF currents through the dielectric material or thermal compound.

In addition to performing as a common-mode decoupling capacitor, a grounded heat sink acts as a Faraday shield when provided with a properly designed mounting fence which surrounds the component's package completely. This Faraday shield also prevents RF currents created from the clock circuitry within the processor from radiating into free space or coupling to other components or internally-routed cable assemblies.

Conclusion

The important concept of routing traces with periodic signals is to provide a properly-terminated, impedance-controlled signal route adjacent to an RF return image plane. Image planes provide for flux cancellation of RF common-mode currents, and allow the trace to function like a coaxial transmission line. Ground vias allow the RF return path to be undisturbed along the entire trace route if multiple ground planes are provided. Otherwise, a ground trace must be used on the routing plane adjacent to the signal trace to assure a constant, undisturbed RF return path.

Different termination methods are available for traces that have fast edge rates and must travel an electrically long distance within a PCB. For each termination method, there are advantages and disadvantages. The termination method that provides optimal performance for most designs is dependent on what the circuit requires. It is important to remember that if a circuit does not function properly in the time domain, frequency domain concerns are moot.

There are various design and layout techniques available which assist with suppression of RF energy within a PCB. Numerous publications describe concepts, yet few provide simple techniques that can be implemented with minimal effort by both design engineers and PCB design-

ers. Only three techniques are presented herein. There are dozens more. It is the desire of this author to make engineers aware of design concepts and layout techniques, along with how they work, in a format that is easy to understand. These techniques are not generally implemented because they are not obvious when one is only concerned with major details during PCB placement and routing.

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