Design and Layout of a Video Graphics System for Reduced EMI

BILL SLATTERY AND JOHN WYNNE
Analog Devices, Norwood, MA

INTRODUCTION

The availability of low cost, high performance video random access memory digital-to-analog converters (RAM-DACs) is a key element in the extension of personal computers into application areas previously considered the preserve of expensive, high-end computer systems. Applications such as computer aided engineering (CAE), computer aided design (CAD), solids modeling, and desktop publishing are becoming more widespread as the cost of the necessary hardware drops. Successfully incorporating a video RAM-DAC into a personal computer or onto a video graphics plug-in board is not difficult once some basic concepts are grasped and some simple guidelines followed (Figure 1).

This article is intended as a guide to the design of a video graphics system in terms of electromagnetic compatibility (EMC). EMC design will be considered as the technique for reducing radiated emissions and electromagnetic interference (EMI) from a high speed video graphics system. EMC implies that the system should not electrically or magnetically interfere with its surroundings, and conversely, the surroundings should not interfere with the operation of the system. In order to provide EMI control in the radio spectrum, government agencies and other international organizations have established limits relating to EMI, most notably Part 15 of the U.S. Federal Communication Commission (FCC) Rules.

Agency certification is the ultimate goal which must be achieved if EMC design is to be considered successful.

This article is divided into a number of sections:

- International EMI Regulatory Bodies — guidelines, testing and radiation limits.
- System Noise Identification — identifying various sources of noise in a system.
- PCB Layout and Design — component placement, multilayer boards, grounding, shielding and filtering components.
- FCC testing for certification.

REGULATIONS CONTROLLING EMI

The ultimate goal which must be achieved if EMC design is to be considered successful is agency certification. In the United States, the Federal Communications Commission is the national regulatory body which sets down strict controls on interference from computing devices. The FCC has divided computer interference into two principal types. The first type, and by far the most demanding of the two, deals with radiated emissions over the frequency range of 30 MHz to 1 GHz. Radiated emissions from personal computers, in a commercial environment, must conform to the limits set for a Class B computing device pursuant to Subpart J of Part 15 of the FCC Rules. Table 1 lists the maximum permissible radiation from such devices, measured in terms of electric field strength.

The second type of emission deals with interference fed back onto the power lines and falls into the Class A category. The FCC conduction limit on this interference is 250 μV maximum (measured according to S15.840 of the FCC Rules) over the frequency range of 450 kHz to 30 MHz. This type of interference is heavily influenced by the design of the switched mode power supply within the computer cabinet. Class C certification, which has less stringent limits, is allowable in certain commercial and industrial applications.

FCC certification is awarded on the submission to the FCC of a complete report, which consists of acceptable test results as well as a detailed description of the test and measurement procedure. Testing has to be carried out by an FCC accredited test laboratory.

A number of international government agencies impose strict criteria on the allowable electromagnetic interference that electronic apparatus can emit. Elec-

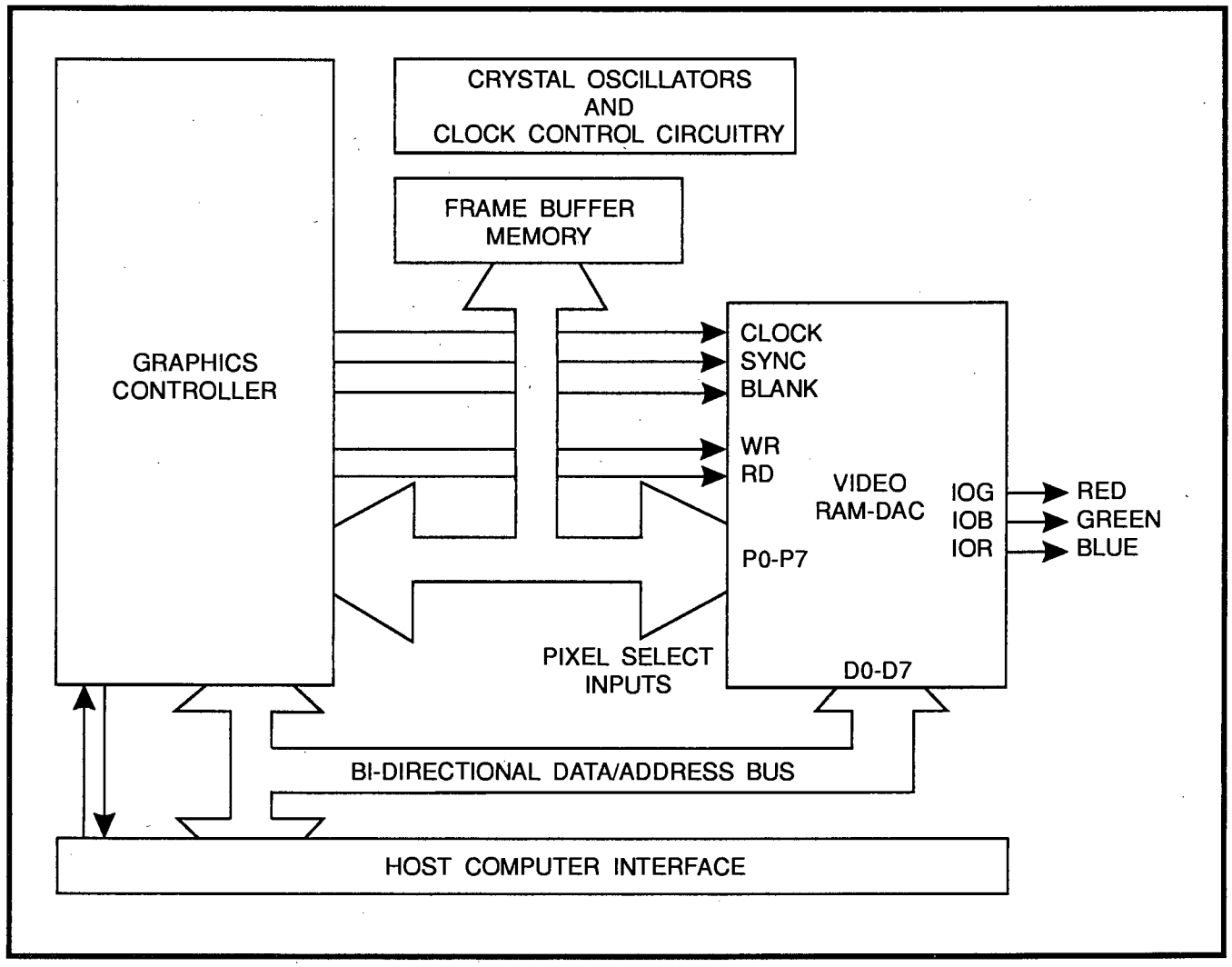

FIGURE 1. *Simplified Block Diagram of a Typical Graphics System Using a Video RAM-DAC.*

FREQUENCY MHz	DISTANCE METERS	FIELD STRENGTH* µV/METER
30 - 88	3	100
88 - 216	3	150
216 - 1000	3	200

** Measured according to S15.840 of the FCC Rules.*

TABLE 1. *Radiation Limits for Class B Computing Devices According to FCC Rules.*

tronic apparatus is required by law to conform to these agency limits, or face severe government penalties. A list of the various international agencies is given in the Recommended Reading section. All agencies have very similar requirements to those of the FCC.

NOISE SOURCES

Identification of noise sources or potential noise sources in a system is the first and probably the most valuable step to achieving a successful EMI design (Figure 2). It may even be possible to eliminate completely a particularly noisy circuit from the design, thus avoiding the later need for filtering. Unfortunately, many possible sources of noise cannot be eliminated from the design, but by being aware of their existence, their effects can be minimized at the source and in the coupling channel by optimum filtering and decoupling. Some of the inherent sources of noise in a video graphics system include:

- Crystal oscillator and clock frequency division circuits.
- Circuits with fast transition times (rise/fall times), e.g., logic families that are unnecessarily fast.
- Unterminated circuits.

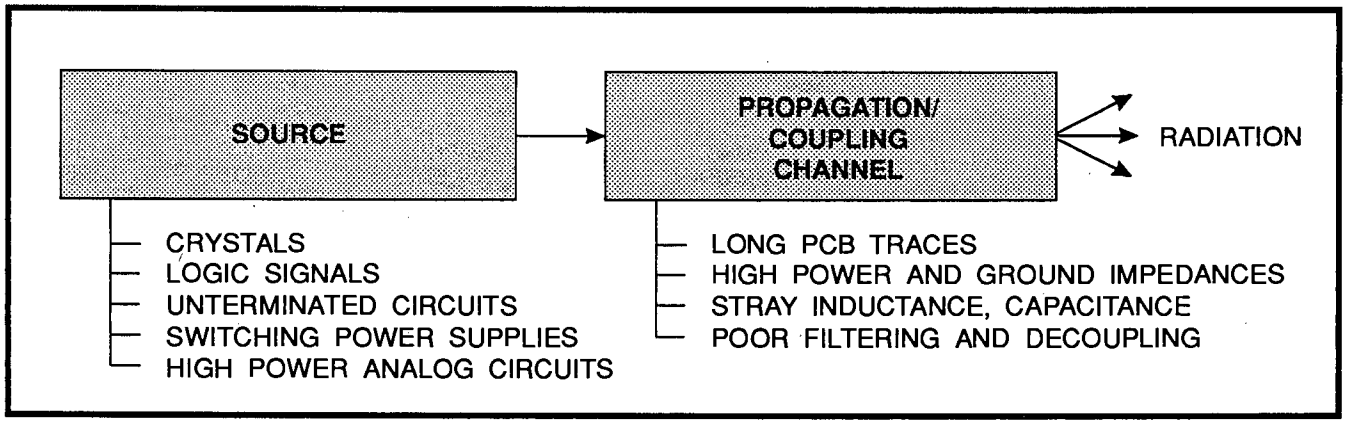

FIGURE 2. *Noise Model of a Video Graphics System.*

- Stray inductances/capacitances.
- Switching power supplies.
- High power analog circuits such as video RAM-DACs.

CRYSTAL OSCILLATORS AND ASSOCIATED CIRCUITRY

A video system usually contains a number of crystal oscillators and associated clock and pixel data circuits which are required to achieve various on-screen pixel resolutions. Some systems have as many as five crystal oscillators varying in frequency from 25 MHz to 65 MHz, and perhaps up to 80 MHz. These crystal oscillators and their associated circuitry tend to be rich in unwanted noise and harmonic components. They can be a prime cause in EMI generation if some basic guidelines are not followed. Some of the important measures are:

- Place crystal oscillator circuits as far as possible from analog circuitry and video output connectors.
- Isolate power supply to crystals through the use of ferrite beads.
- Avoid the mixing of clock buffers and other logic in the same IC package.

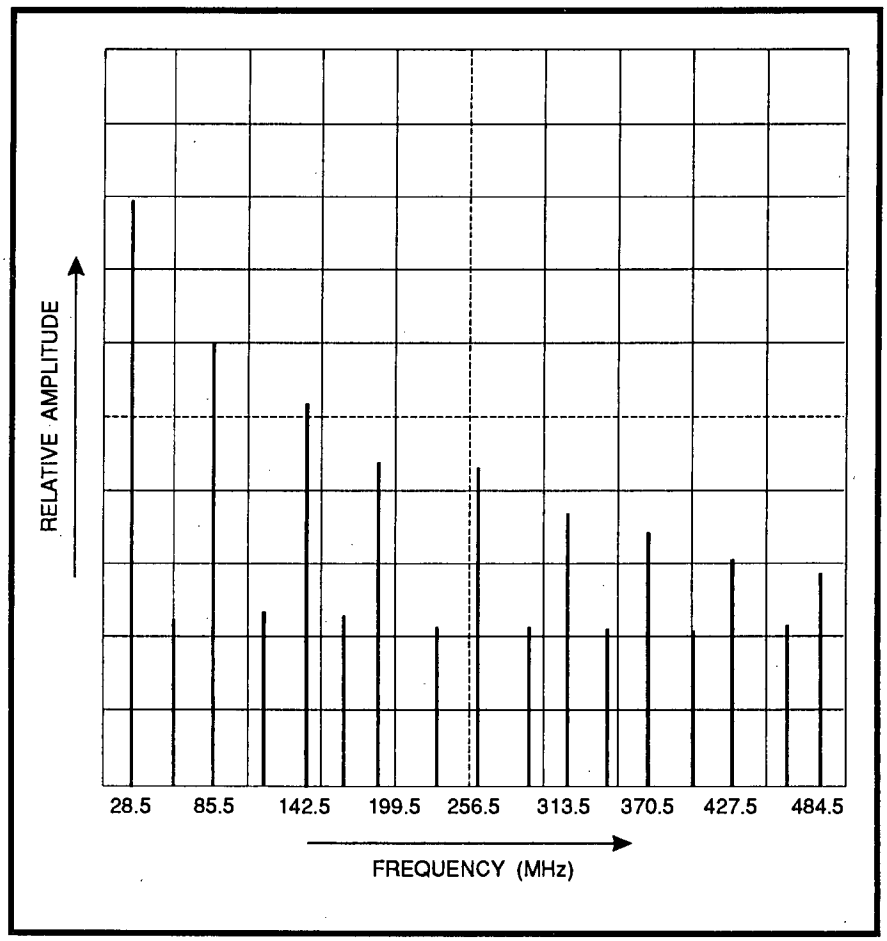

FIGURE 3. *Magnitude of Harmonic Components Relative to the Fundamental for a 28.5 MHz Crystal Oscillator.*

- Use several low power data drivers or buffers for clock and pixel data lines distributed throughout the board, rather than a single high power driver.

With regard to the crystal oscillators themselves, the critical aspects which must be considered include the wave shape and the transition time (rise/fall time). Figure 3 is a plot of the output frequency spectrum of a typical 28.5 MHz crystal oscillator. It shows the amplitude of the harmonic components relative to the fundamental. It can be clearly seen that although the crystal's fundamental frequency lies outside the FCC's lower limit

of 30 MHz for radiated EMI, higher-order harmonic components exist throughout the FCC-controlled band. The frequency of the crystal oscillators should be kept to the required minimum, and transition times should be kept as slow as possible. This reduces the amplitude of unwanted harmonics, while still satisfying system functional performance needs.

TECHNOLOGY	IC FAMILY	TRANSITION TIME
TTL	74	10 ns
	74LS	12 ns
	74ALS	3 → 20 ns
	74S	6 ns
	74AS	2 → 9 ns
	74F	1.2 → 8 ns
CMOS	74HC	20 → 150 ns

TABLE 2. *Comparison of Transition Times for IC Logic Families.*

The clock circuitry, which includes crystal oscillators and pixel data lines, is the primary source of most system noise. Keeping this circuitry as far and as isolated as possible from other circuitry, especially analog circuitry, is important. On the other hand, it could be argued that running long pixel data and clock lines from such circuitry to the video RAM-DAC in itself is not desirable. Long lines increase noise coupling to other parts of the system. A trade-off between the length of pixel lines and the placement of high speed clock circuitry must be considered. The designer must attempt to optimize these two competing goals. As mentioned earlier, the use of multiple low power buffers helps to ease such a conflict. A distance of less than three inches between buffers would be desirable in such circumstances.

OTHER NOISE SOURCES

A number of other noise generators can be easily identified. Circuits with fast transition times, including memory chips, logic circuitry and the graphics controller, all contribute to the overall noise of the system. The faster the signal transition time, the greater the amplitude of the resulting harmonics, as was seen in the previous section relating to crystal oscillator circuits.

As a general rule, devices with the slowest possible rise/fall times that will achieve the system's tasks should be used. Table 2 lists some typical rise/fall times for various logic families.

Stray inductances and capacitances can cause signals to ring, to overshoot, or to undershoot the steady state voltage levels. This ringing is a source of EMI which can be minimized by keeping wires or traces short and adding a series of damping resistances at the source or termination of long signal paths. Also, unterminated circuits with floating signal lines should be avoided, because these can result in unwanted oscillations.

Power to all devices of a system is usually derived from switch-mode power supplies. While the design of the power supply is critical to the reduction of conducted noise in the band of 450 kHz up to 30 MHz, harmonics generated by the switching power supplies can extend well into the radiation frequency band and thus add to EMI.

Modern high resolution color graphics monitors are driven directly by analog signal levels from the DACs. The relatively high power, analog output levels from the red, green and blue current sources of the video DAC require careful attention. As will be discussed in the PCB layout section, the power to the video RAM-DAC should be isolated from the remainder of the PCB power plane. If noise on the high speed pixel and clock input section to the video RAM-DAC has not been minimized, noise will be coupled through to the analog output section and onto the connecting cable to the monitor, causing this cable to act as an antenna. If necessary, filtering at the source termination of each of the three DAC outputs can be used to further minimize the noise.

PRINTED CIRCUIT BOARD DESIGN

The extent of radiated emissions from a printed circuit board (PCB) will be determined by the ability of the PCB to act as a propagation channel for unavoidable noise sources, its ability to couple this noise onto other circuitry, and the radiation into free space of this undesired noise. Aside from a PCB's ability to radiate EMI, noise coupled from digital circuits on the board to the video RAM-DAC can adversely affect the system's functional performance.

CAUSES OF EMI

The main sources which conduct or radiate EMI from a printed circuit board are as follows:

- Common impedance coupling

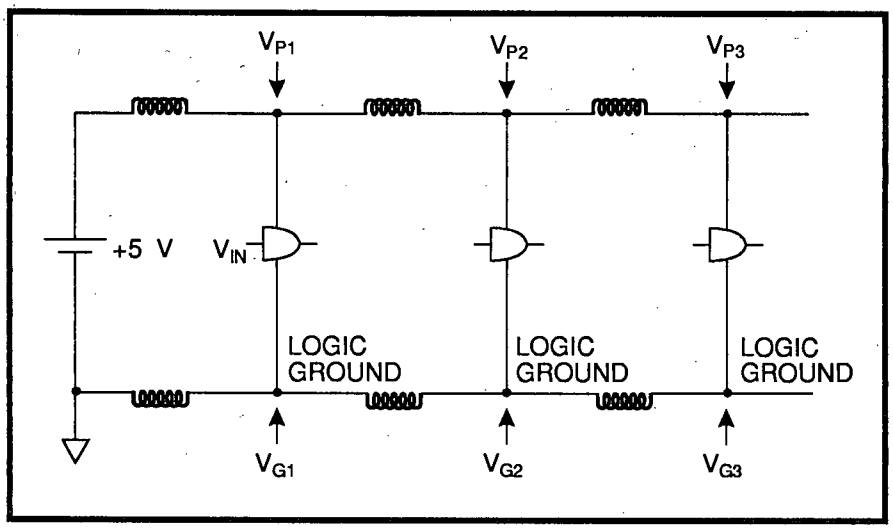

FIGURE 4A. *Common Impedance Coupling via Power and Ground Traces.*

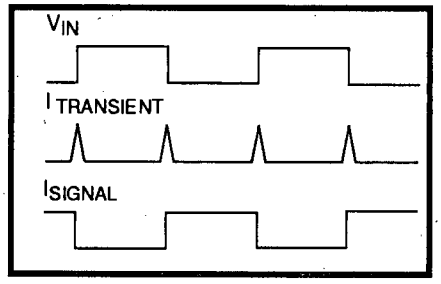

FIGURE 4B. *Signal and Transient Currents Due to Gate Switching.*

via power and ground traces.

- Antenna loops formed by ICs and their bypass capacitors. Note that these loops also include the power and ground lead frame members within the IC packages.
- Printed circuit board traces carrying signal currents. Note again that signal lead frame members within the IC packages are also included.
- Crosstalk between adjoining signal traces.

COMMON IMPEDANCE COUPLING

An example of common impedance coupling via power and ground traces is shown in Figure 4A where a number of logic gates are supplied with power over common printed circuit board traces. A typical V_{IN} input signal to one of these gates is shown in Figure 4B. The resulting transient and signal currents due to the gate switching are also shown.

The distributed trace inductances act as impedances to these switching currents and spread the resulting high frequency noise to all nodes common to the culprit. The magnitude of the generated high frequency noise is shown in Figure 5A. The associated worst signal current for a standard transistor-transistor logic (TTL) gate is shown in Figure 5B.

Consider the harmonic components present in the switching signal current of Figure 5B. This assumes the gate is driving 10 standard TTL loads with a maximum sink current of 16 mA and a maximum source current of 0.4 mA.

With a mark/space ratio of τ/T and using a Fourier Series expansion, the formula for the amplitude of the nth harmonic is given by:

$$I_n = \frac{2A\tau}{T}\left[\frac{\mathrm{Sin}\left(\frac{n\pi\tau}{T}\right)}{\frac{n\pi\tau}{T}}\right]$$

where n = 1, 2, 3 ...

For a square wave $\tau/T = 0.5$, the amplitude of the third harmonic (n = 3) is:

$$I_3 = 3.4 \text{ mA, zero to peak}$$

At 28.5 MHz, the magnitude of the impedance of the ground trace in Figure 5 is given by:

$$Z = [2\pi fL]$$

where

f = 28.5 MHz, and
L = 20 nH/inch (typically).

Hence, Z = 3.58 Ω/inch.

At 85.5 MHz (3 · 28.5 MHz) the impedance is 10.74 Ω/inch. Thus, the high frequency voltage at the logic ground node of the switching gate due to the third harmonic alone is equal to:

$$V_{G1} = (3.4 \cdot 10^{-3})(4)(10.74) \text{ V}$$
$$= 146 \text{ mV peak at 85.5 MHz}$$

This high frequency component and other similar components will be circulated around the printed circuit board via the common ground traces. It will also appear on any cable shielding attached to this common ground trace, and depending on how efficient the cable shield is as an antenna, will be radiated into free space.

ANTENNA LOOPS

One of the most important principles of PCB layout and design for noise reduction can be described by the directive: *Minimize Signal Loop Areas.*

In most circuit designs, the currents are thought of in terms like flowing "out" of one place, "through" some other place and "to" the target point. Unfortunately however, a consideration of how these currents will eventually find their way back to their source is neglected. Ground and

supply voltage points are considered "equivalent," and the fact that they are parts of a network of conductors through which currents flow and develop finite voltages is often not appreciated. These voltages can radiate to cause EMI (Figure 6). Voltages are generated because, as a result of inherent inductances, wires and traces do not have zero impedance.

Many of the problems associated with power and ground loops can be avoided through the employment of effective bypassing techniques. The aim of effective bypassing is to maximize the charge stored in the bypass loop while simultaneously minimizing the inductance of this loop. Inductance in the loop acts as an impedance to high frequency transients and results in power supply spiking. Figure 7A shows a poor bypass arrangement. The associated inductances due to the large loop area are illustrated in Figure 7B.

In addition to loop inductances, the series inductance of the bypass capacitor itself must also be considered. It is well known that there is more inside a capacitor's body than a pure capacitance.

The simplified equivalent circuit of a 0.1 µF capacitor in Figure 8 shows an effective series resistance (ESR) and effective series inductance (ESL) in series with the ideal 0.1 µF capacitance.

Figure 9 shows the complete inductive loop associated with the bypass circuit. These inductances increase the total series inductance of the bypass loop and hence lower the series resonant frequency as determined by the equation:

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

Above the series resonant frequency the impedance becomes more inductive, increasing linearly with increasing frequency. For instance, a 0.1 µF ceramic radial lead capacitor with 1/4-inch leads generally resonates around 10 MHz.

The minimum value of the bypass capacitor required is determined by the maximum amount of voltage drop allowable across the capacitor as a result of the transient current. An approximate value for a bypass capacitor is given as:

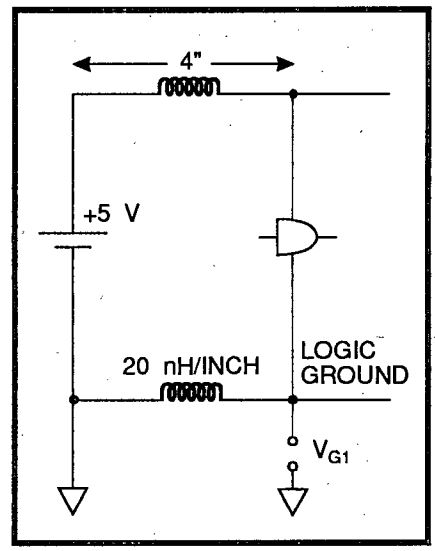

FIGURE 5A. *Common Impedance Coupling Due to One Gate.*

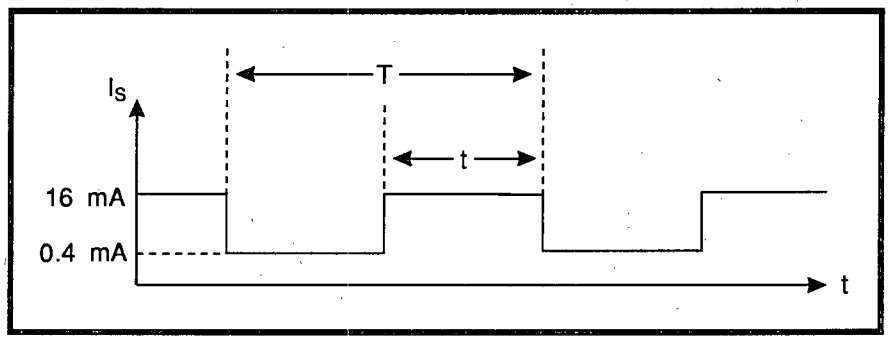

FIGURE 5B. *Signal Current Due to TTL Gate Switching.*

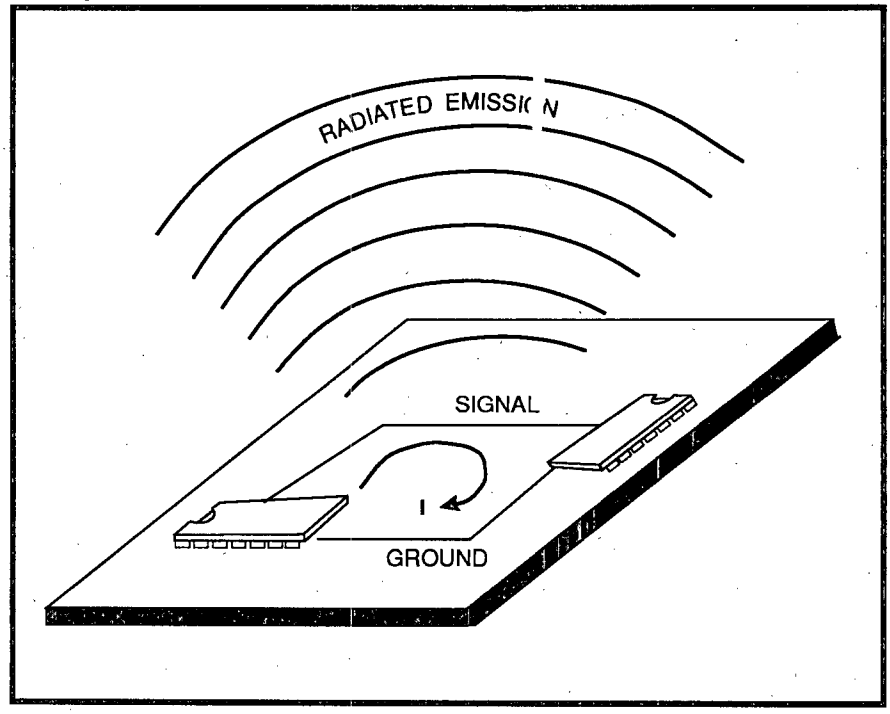

FIGURE 6. *Currents Flowing in Large Loops Add to EMI.*

$$C = \frac{I.\Delta\tau}{\Delta V} \text{ Farads}$$

where

I = Maximum transient current
$\Delta\tau$ = Transient duration
ΔV = Allowable voltage drop

For example, a typical 74 HC I_{CC} transient is 20 mA high and lasts 20 ns. If the voltage drop is to be kept below 100 mV, then the required bypass capacitor is:

$$\frac{(20 \text{ mA})\ (20 \text{ ns})}{(100 \text{ mV})}$$

or 4 nF per output.

However, any series inductance in the bypass loop will cause additional voltage spiking. For any given magnitude of noise spike, an approximate expression for the maximum amount of series inductance is given by:

$$L = \frac{V.\Delta\tau}{\Delta I} \text{ Henrys}$$

where

V = Maximum noise spike
$\Delta\tau$ = Transient duration
ΔI = Transient current

The typical 74 HC I_{CC} transient of 20 mA has a rise/fall time of 4 ns. Thus, if the inductive noise spike is restricted to 100 mV peak, the maximum amount of series inductance is:

$$\frac{(100 \text{ mV})\ (4 \text{ ns})}{(20 \text{ mA})}$$

or 20 nH.

Referring back to Figure 9, this means that the combined total of ESL, L_L, L_{PC} and L_{IC} must be kept below 20 nH. To a greater or lesser extent the first three terms are within the PC board designer's influence; the fourth term, the inductance of the IC lead frame member, or L_{IC}, is invariable, as it is determined by the IC package. The use of PLCC packaged parts inherently reduces L_{IC} to 2-3 nH as against 10-12 nH for the more traditional DIP parts.

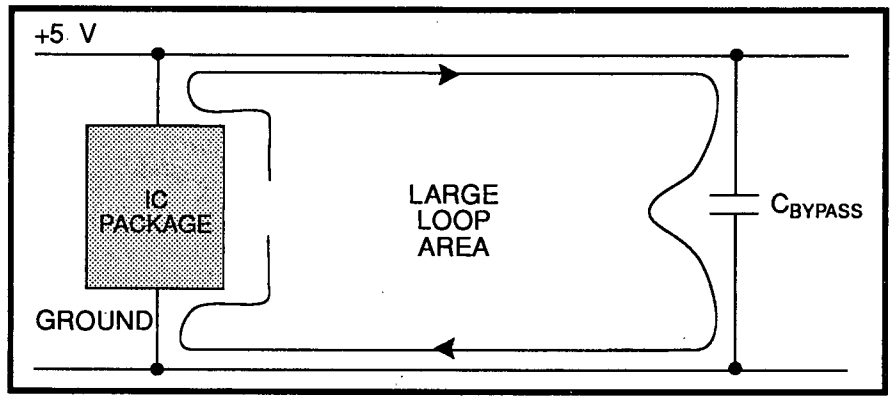

FIGURE 7A. *Large Loop Associated with Poorly Placed Bypass Capacitor.*

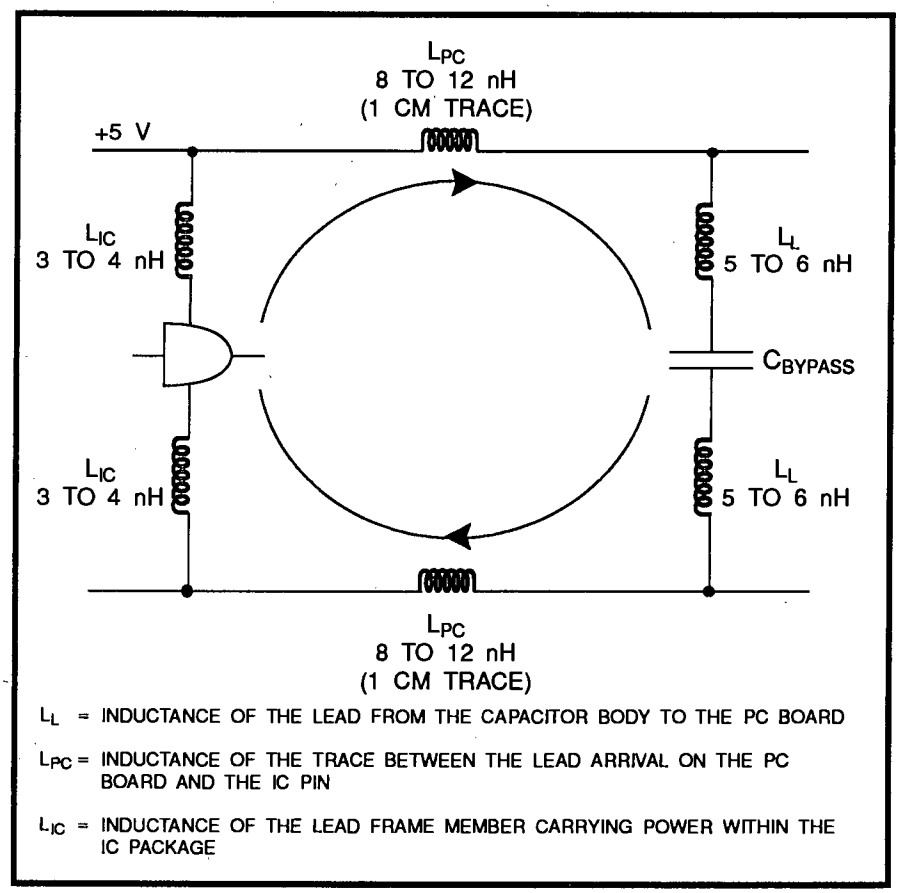

FIGURE 7B. *Equivalent Circuit of Bypass Loop of Figure 7A.*

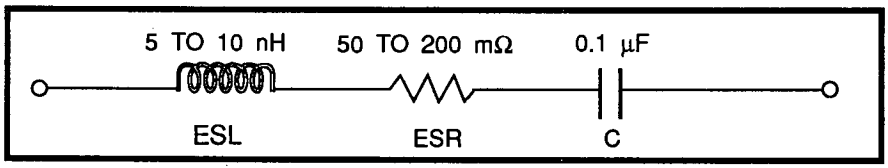

FIGURE 8. *Equivalent Series Representation of a Bypass Capacitor.*

MULTILAYER PC BOARDS

In the design of a high performance, high speed graphics system, a four-layer printed circuit board is recommended.

Figure 10 shows a cross-sectional view of a four-layer printed circuit board, with power and ground planes separating the signal-carrying traces of the component and solder sides of the

PCB. Consideration should be given to the use of multilayer boards and the relevant placement of components. Figure 11 shows a suggested component placement scheme.

POWER AND GROUND PLANES

Power supply decoupling attempts to contain the transient currents within the bypass loop. However it cannot be 100-percent successful, and some high frequency components will escape onto the power and ground traces. High frequency signal currents will also be flowing in the power and ground traces. In order to avoid common impedance noise coupling due to these currents, it is necessary to reduce the impedance of the power and ground traces to an absolute minimum. The only satisfactory way to achieve this is not to use traces at all but to use power and ground planes. On a PC card-sized, two-layer board with one side devoted to a ground plane, the impedance of the plane is in the tens of milliohms range.

A four-layer board allows another plane to be used as a power plane. Low impedance power and ground contacts are thus available over the full area of the board. Additionally, in a four-layer board with power and ground planes inside the board and signal traces on the top and bottom of the "sandwich," overlapping power and ground planes act as inherent distributed capacitors (Figure 10). This provides some measure of high frequency decoupling. The major advantage of using a ground plane is the very substantial reduction in signal loop area it provides. In a typical PCB layout, signal current flows out through one trace and back through a ground trace. Such a path can include a large loop area. A large loop area, as has already been discussed, implies high inductance for the traces with subsequent signal ringing, EMI radiation and crosstalk. To reduce the inductance it is necessary to reduce the loop area through which the signal current flows. The use of power and ground planes minimizes loop areas, thereby reducing inductances and resultant EMI.

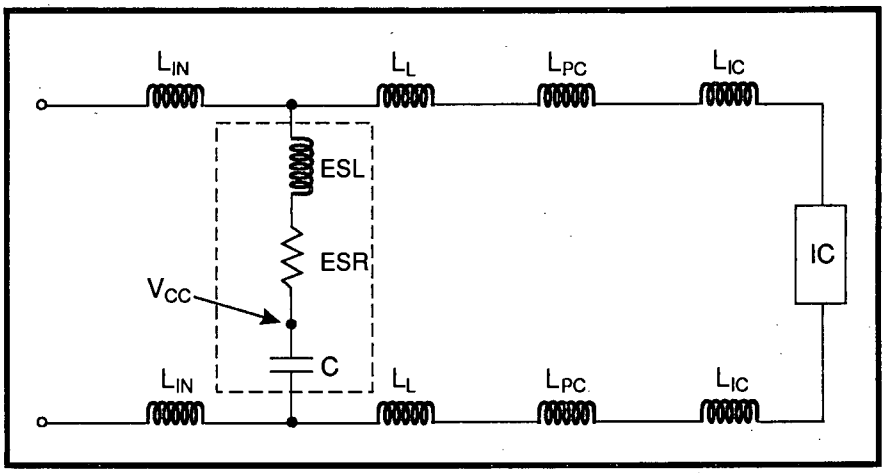

FIGURE 9. *Inductive Loop of a Bypass Circuit.*

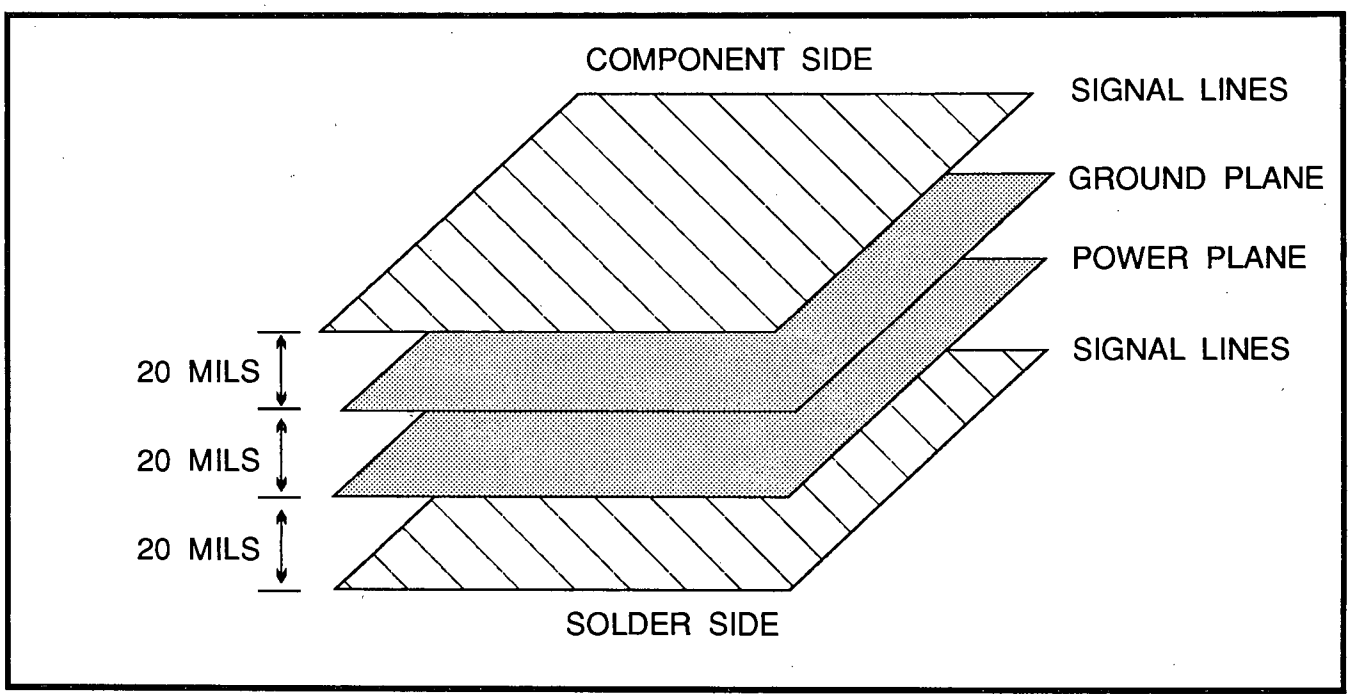

FIGURE 10. *Four-layer Printed Circuit Board Construction.*

The electromagnetic fields associated with an idealized case of two parallel wires carrying equal and opposite currents are shown in Figure 12.

The two fields (electric, E, and magnetic, H) tend to be confined between or near the conductors. The electric field is strongest in the plane of the conductors. The magnetic field is nonzero at points close to the conductors, but farther away (relative to the wire spacing) the fields from both conductors tend to cancel out. Keeping the conductors together promotes field cancellation, which can be viewed either as minimizing the loop area or minimizing the inductance; the results are the same.

Introducing a ground plane (sheet of copper) halfway between the wires, as shown in Figure 13, does not disturb the field pattern even when the lower wire is removed. A virtual image of the lower wire has been produced in the copper plane to maintain the original field configuration. This is the basis of microstrip. With a properly designed ground plane system, the return current will always flow under the signal trace, the path of lowest impedance.

DIGITAL SIGNAL INTERCONNECTIONS

The use of a ground plane allows the signal interconnects to be viewed as microstrip transmission lines whose characteristic impedances, propagation delays, etc., can be readily calculated. Microstrip is the name given to a transmission line which consists of a signal trace separated from a ground plane by a dielectric. Figure 14 shows the cross-section of such a line.

The characteristic impedance, Z_o, of this line is:

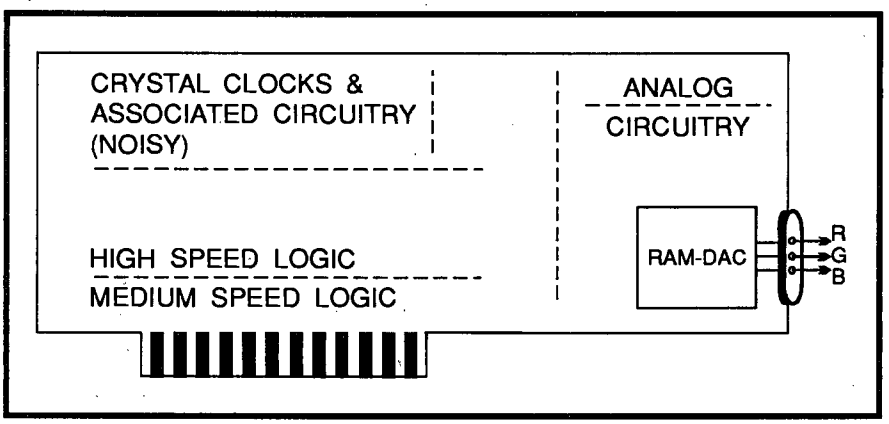

FIGURE 11. *Printed Circuit Board Component Placement.*

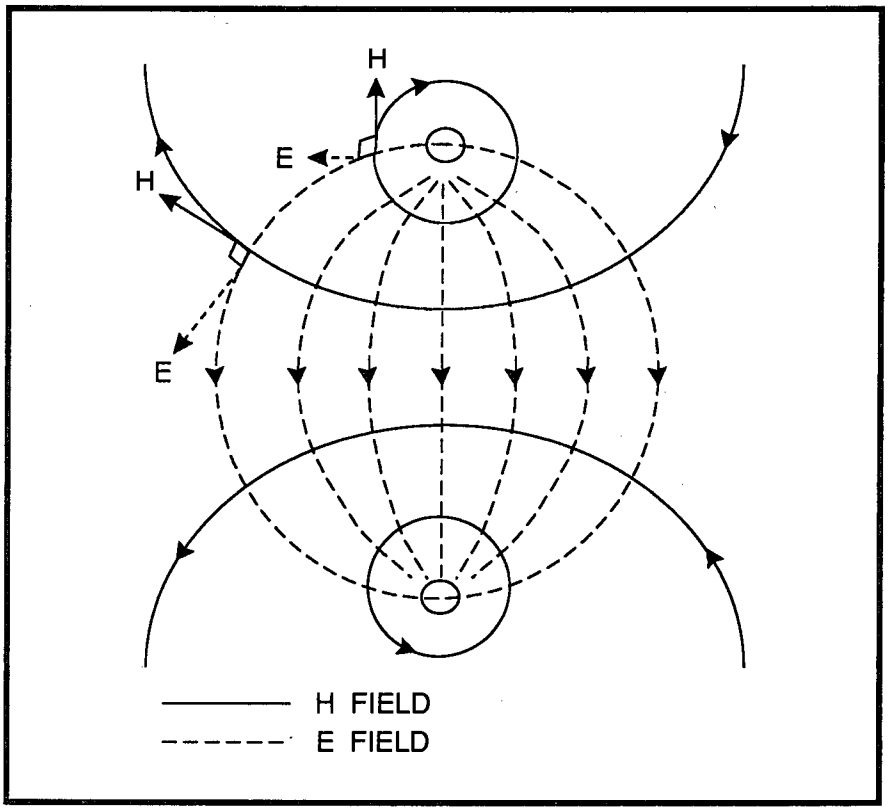

FIGURE 12. *Electromagnetic Field Around Two Parallel Conductors Carrying Equal and Opposite Currents.*

$$Z_O = \frac{87}{\sqrt{\varepsilon_R + 1.41}} \text{Ln}\left\{\frac{5.98\ h}{0.89\ b + c}\right\} \Omega$$

where

ε_R = Relative dielectric constant of board.

Typically, $\varepsilon_R = 5$ for glass/epoxy boards, and b,c,h = the dimensions indicated in Figure 14. The propagation delay, t_{PD}, of a microstrip line is given by:

$$t_{PD} = 1.017 \sqrt{0.475\ \varepsilon_R + 0.67}\ \text{ns/ft}$$

Note that this propagation delay is dependent only on the dielectric constant and not on the line geometry.

Figure 15 shows impedance values for various configurations of microstrip lines.

Gross impedance mismatches between the transmission line's

characteristic impedance and the source (driver output) or load (receiver input) impedances connected to the line reflect the signal back and forth on the line. These reflections will cause overshoot, EMI radiation and crosstalk. By properly terminating the line with either source or load impedances which match that of the transmission line, reflections can be eliminated or substantially reduced. However, not every signal interconnect demands line termination; the need is determined by the relationship between the rise (or fall) time of the signal and the time required for the signal to travel the length of the interconnect. As a general guideline for digital signals, line termination is needed if the one way propagation delay, t_p, over the length of the interconnect is greater than 1/8 of the signal rise time, t_R. That is, line termination is needed if:

$$t_P \geq (1/8) \cdot t_R \text{ secs}$$

A number of dc and ac termination techniques exist which trade increased power dissipation against component count. The simplest termination technique which dissipates no extra power is a series termination in which a resistor is placed in series with the signal interconnect at the source end of the line (Figure 16). The resistor should have a value equal to the characteristic impedance of the line minus the output impedance of the driver, and should be of metal-film construction or some other low inductance material. The load impedance is considered an open circuit. Series termination is most suitable for systems where only one receiver is connected to the line. Note that if pull-up resistors are required on digital or clock signals, they should be connected to the PCB power plane (V_{CC}).

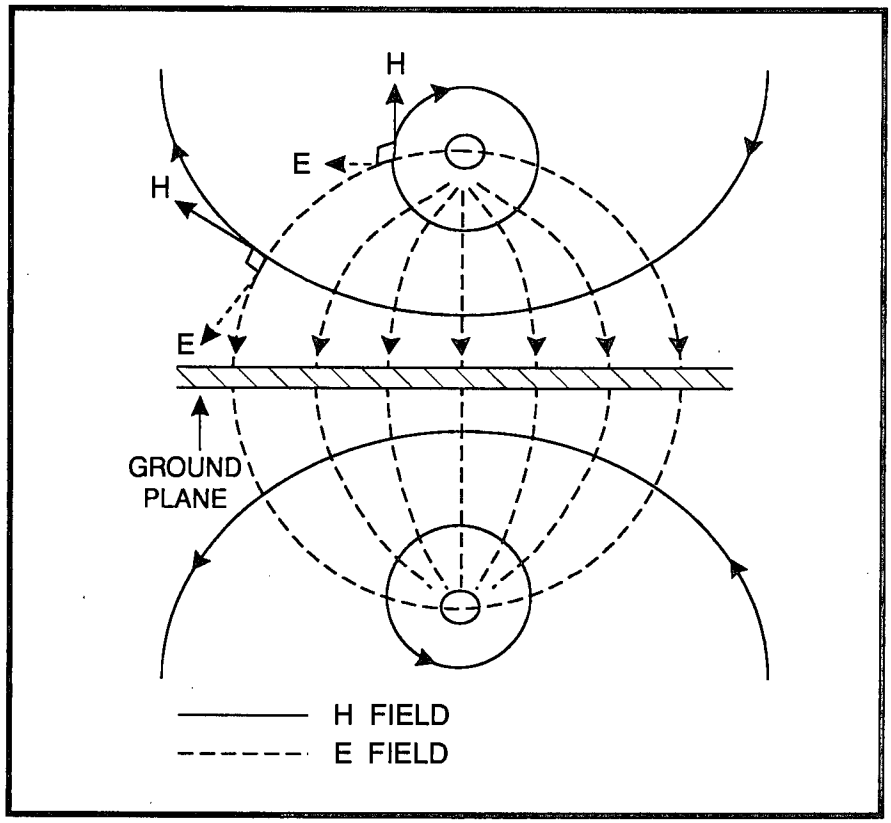

FIGURE 13. *Electromagnetic Field Around Two Parallel Conductors Separated by a Ground (Copper) Plane.*

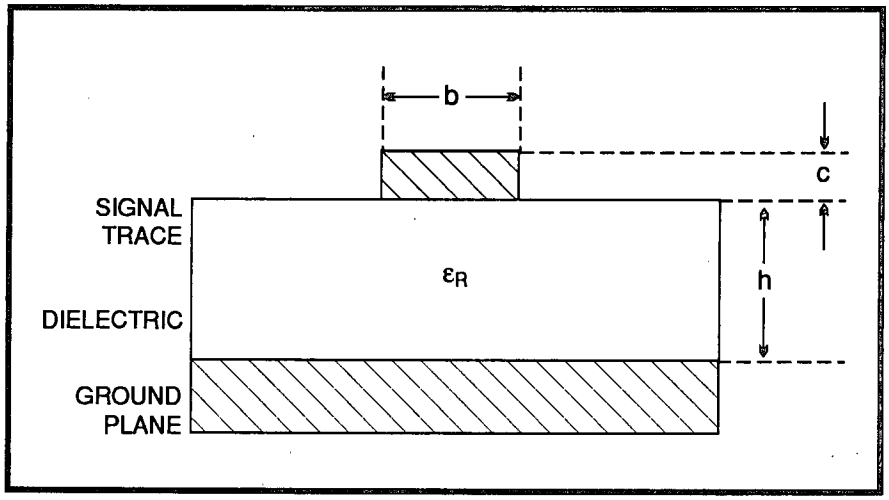

FIGURE 14. *Cross-section of Microstrip Transmission Line.*

CROSSTALK

Crosstalk is any unwanted signal coupling between parallel PC-board traces due to mutual inductance (L_M) and capacitance (C_M) (Figure 17).

In general, crosstalk is directly proportional to line impedances, frequency and line lengths and inversely proportional to line spacing. Much of the induced crosstalk in a signal line is from immediately adjacent transmission lines, which suggests that wider spacing between lines will reduce the problem. This may

not always be possible in closely spaced circuits, so an alternative approach is to shield the signal lines by inserting narrow grounded traces between each signal line on the same wiring plane (Figure 18).

At high frequencies, capacitive coupling dominates. The addition of a shield (or ground trace) between the signal lines changes the equivalent circuit. Crosstalk is now reduced since the inductance, L_M, is now much larger than either L_1 or L_2 and capacitance, C_M, is much smaller than either C_1 or C_2.

SEPARATE POWER PLANE FOR VIDEO RAM-DAC

To further isolate the video RAM-DAC from the PCB's power supply, V_{CC}, a separate power plane, V_{AA}, is recommended for the video RAM-DAC and its associated circuitry. This analog power plane should be connected to the regular PCB power plane, V_{CC}, at a single point through a suitable filtering device such as a ferrite bead (Figure 19). This ferrite bead should be located no more than three inches away from the video RAM-DAC. In the case of multiple power, V_{AA}, pins, it is important to connect all V_{AA} pins to the analog power plane. This eliminates any possibility of latch-up in the device.

COMMON GROUND PLANE

Due to the presence of RAM on some graphics boards, isolating the device's ground circuitry from the main PCB ground is not recommended. Corruption of data could occur. These video RAM-DACs should have all ground pins connected to the PCB's regular ground plane.

ANALOG OUTPUTS

The analog outputs of some video RAM-DACs are driven by switched current sources. These parts are designed to drive either a singly or doubly terminated 75 Ω load. The doubly terminated configuration shown in Figure 20 is the preferred choice.

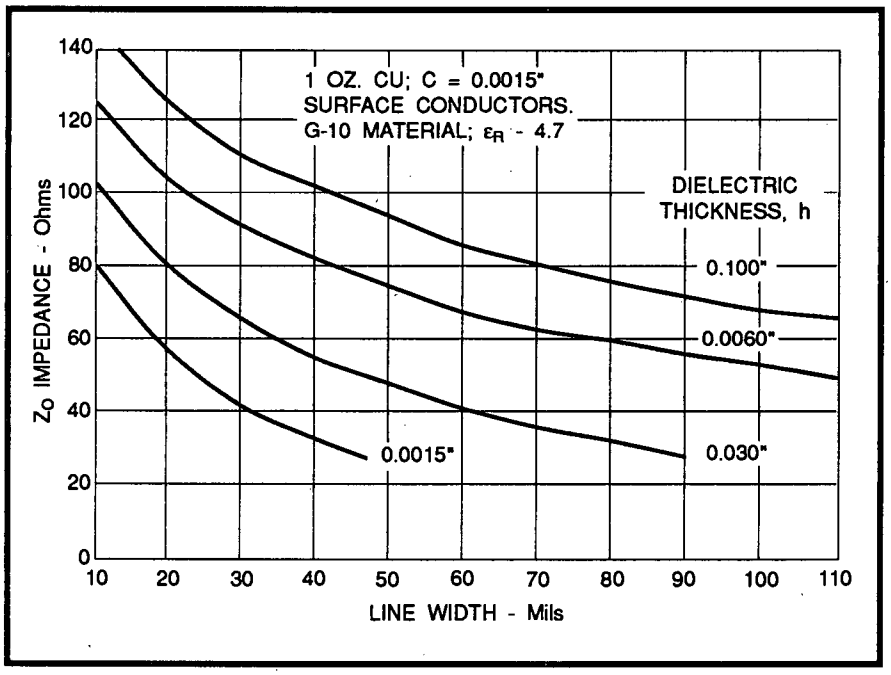

FIGURE 15. *Impedance Versus Line Width and Dielectric Thickness for Microstrip Lines.*

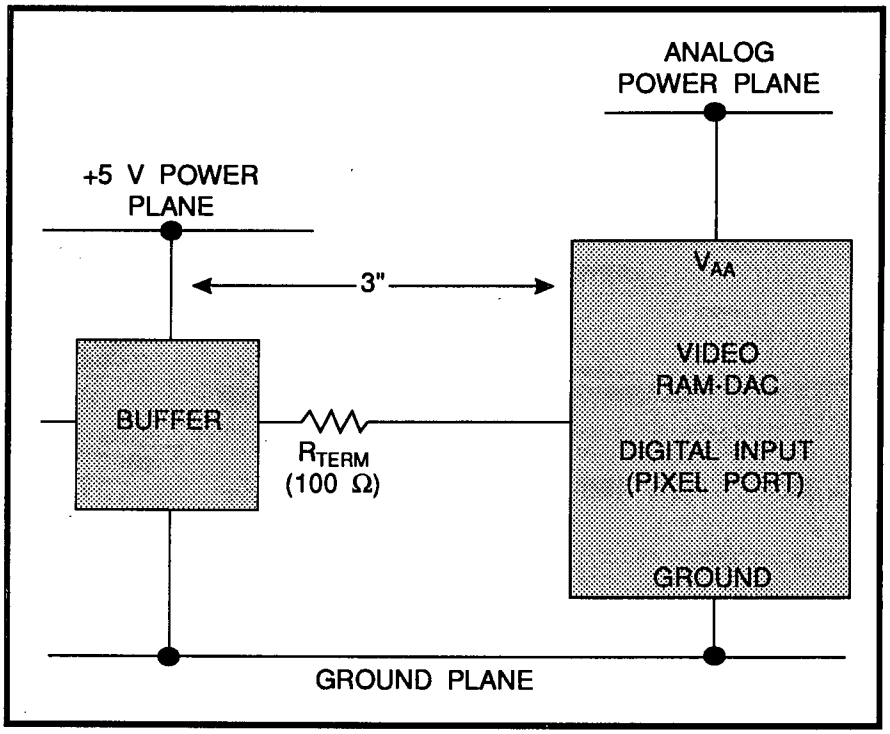

FIGURE 16. *Series Termination of Signal Lines.*

DAC output traces on a PCB should be treated as transmission lines. It is recommended that the video RAM-DAC be placed as close as possible to the output connector, with the analog output traces being as short as pos-

sible (less than 3 inches). The 75 Ω termination resistors should be placed as close as possible to the DAC outputs and should overlay the PCB's ground plane. Also, short analog output traces will reduce noise pick-up and minimize reflections due to neighboring digital circuitry.

SURFACE MOUNT TECHNOLOGY (SMT)

Surface mount technology (SMT) offers many EMI advantages over traditional through-hole designs. Because SMT features smaller component sizes and allows the designer to place components on both sides of the printed circuit board, it provides superior PCB integration. This means that loop lengths can be reduced and noisy signal traces can be shortened, all having a positive effect on EMI. The shorter lead lengths of SMT packages decrease inductance, thereby providing better high frequency performance.

Most components required for a video graphics system are available as surface mount devices. Memories, controller chips and logic are all available in small SMT packages. Resistors and capacitors can also be purchased in a small "chip" format.

GETTING FCC CERTIFICATION

The final chapter in EMI design is the actual test. With good design practice and adherence to some of the issues raised in this article, no difficulty should be encountered in achieving certification. However, the testing itself must be carried out with great care in order to do justice to a design. It should be remem-

Continued on page 102

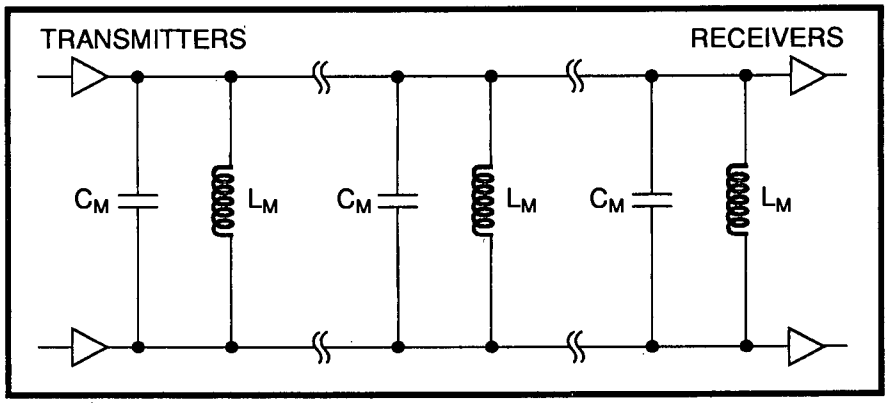

FIGURE 17. *Capacitive and Inductive Coupling Between Signal Traces.*

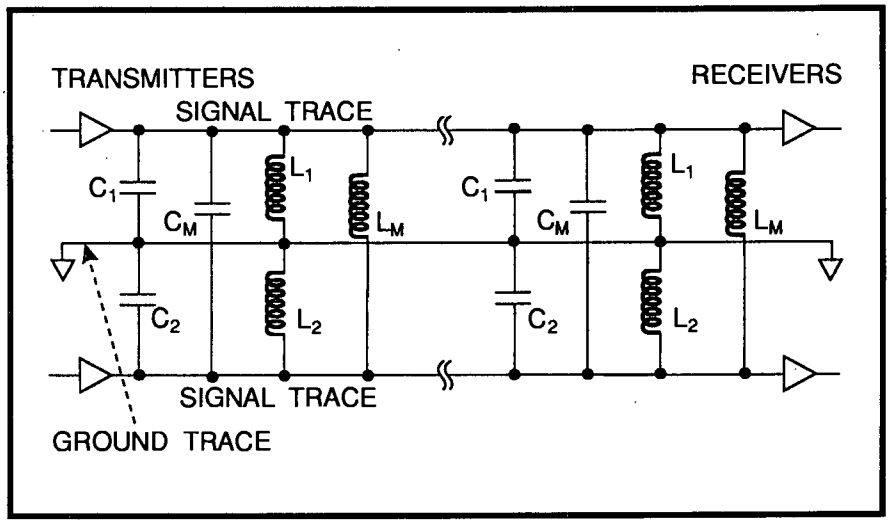

FIGURE 18. *Ground Trace Between Signal Lines Reduces Crosstalk.*

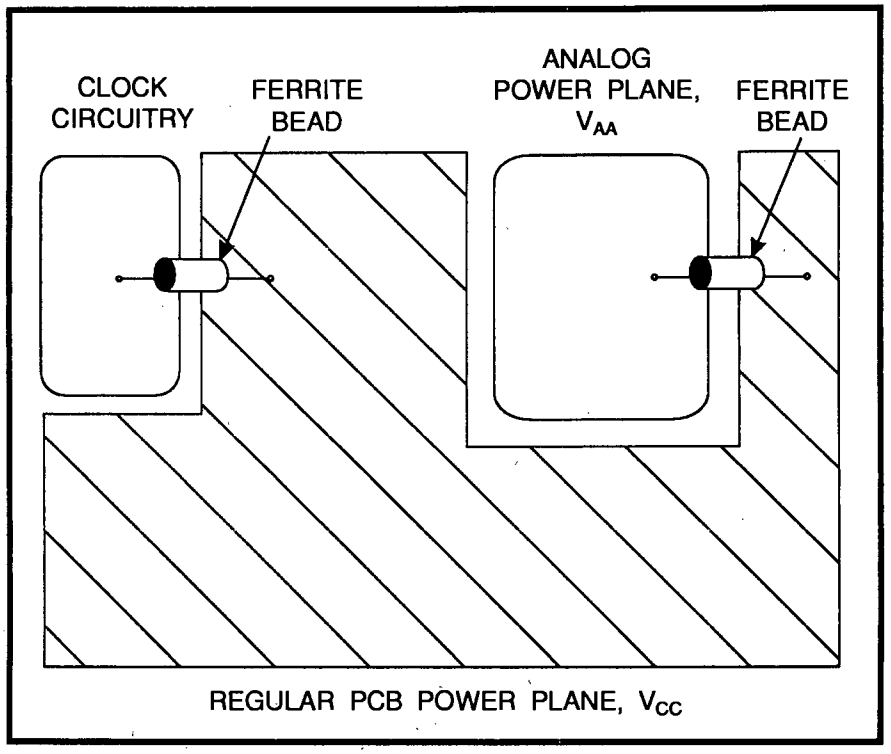

FIGURE 19. *Power Plane Decoupling Using Ferrite Beads.*

base and sporadic adhesion problems.

VACUUM DEPOSITION

Vacuum deposition can be very cost-effective. However, long-term reliability in resistance to aging is a problem. As a result, vacuum deposition has achieved only marginal acceptance by computer manufacturers.

CONCLUSION

Of the available shielding technologies, copper conductive paints have made the most dramatic advances. They have displaced nickel paint in performance areas and now offer a technologically viable cost-effective alternative for single and double-sided plating. Nevertheless, the features and benefits of each alternative should be examined in terms of the specific enclosure to determine the optimum shielding technology.

ROY W. BJORLIN *is Business Manager, Conductive Coatings Group for Spraylat. Mr. Bjorlin joined the conductive coatings group in 1989 and has fifteen years of experience with business development of thick-film coating technologies, discrete packaging, component manufacturing and chemical process systems for shielding. (914) 699-3030.*

BRUCE K. BACHMAN *is Product Manager, Conductive Coatings, Western States. Mr. Bachman joined the conductive coatings group in 1990 and has thirteen years of experience in plating technologies, including memory disks, specialty stripping, gas turbine engines, plating-on-plastics, and EMI/RFI for composites and non-conductors. (619) 482-2339.*

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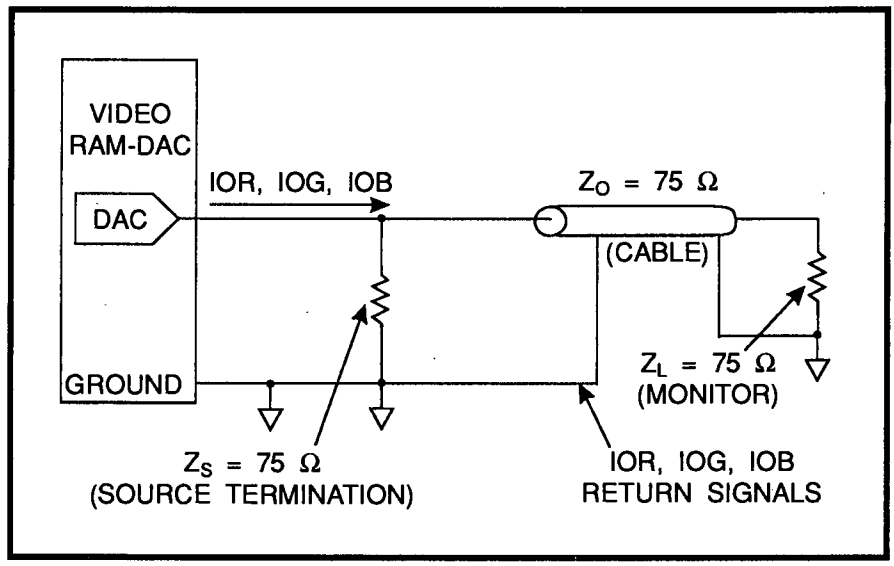

FIGURE 20. *Recommended Analog Output Termination for Video RAM-DACs.*

bered that in the case of a peripheral device, FCC testing is applied to a *complete* operating computer system.

A complete operating computer system is comprised of the following: A PC compatible computer with keyboard; a printer connected to the printer port; a mouse or modem connected to the serial port; and a monitor. The PC and all its peripherals must be operating when measurements are made.

It is paramount that only the best equipment be used. If, for example, a noisy monitor is used, the test results might not pass all the agency limits, not because the board is at fault, but perhaps because of a poor quality, noisy monitor used in the test. Another principal culprit causing EMI in such a system is the parallel printer cable. A good quality shielded cable must be used. Also, if an outside test house is used, a representative from the company should be on hand who understands the operation of the system and its various components.

RECOMMENDED READING

Brokaw, Paul A., "An IC Amplifier Users' Guide to Decoupling, Grounding and Making Things Go Right for a Change," *Analog Devices Data-Acquisition Databook* 1984, Vol. 1, pp. 20-13 to 20-20.

EMI Countermeasures — Application Guidance, Murata Manufacturing Co. Ltd.

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Motorola, Inc., *MECL Design Handbook*, 2nd Edition, 1972.

Ott, Henry W., *Noise Reduction Techniques in Electronic Systems*, John Wiley, NY, 1986.

BILL SLATTERY *is a senior engineer with the computer graphics and video applications group at Analog Devices in Ireland. He has been with Analog Devices since 1986, when he graduated from University of Dublin (Trinity College) with a BSC in Electrical Engineering. 353 61 29011 ext. 343.*

JOHN WYNNE *is application engineering manager at Analog Devices in Ireland. Previously he was a designer at Sperry Gyroscope's Avionics Division in the United Kingdom. He has published a large number of articles in various publications. 353 61 29011 ext. 141.*