EMI SUPPRESSION UTILIZING MLC DISCOIDAL ARRAYS

INTRODUCTION

The FCC rules for computing devices place stringent limits on the radio frequency emissions generated by electronic computing equipment. Radio frequency energy can be conducted or radiated from almost any part of electronic equipment and very little needs to be lost into space in order to exceed the FCC regulations. (See Figure 1.) For example, emissions as low as 1×10^{-3}

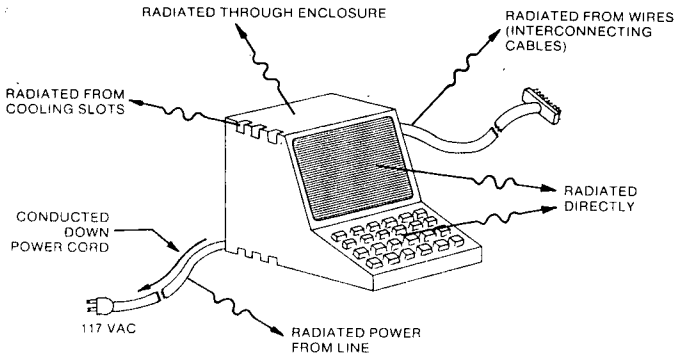

Figure 1. Energy can be conducted and radiated from any part of the system.[1]

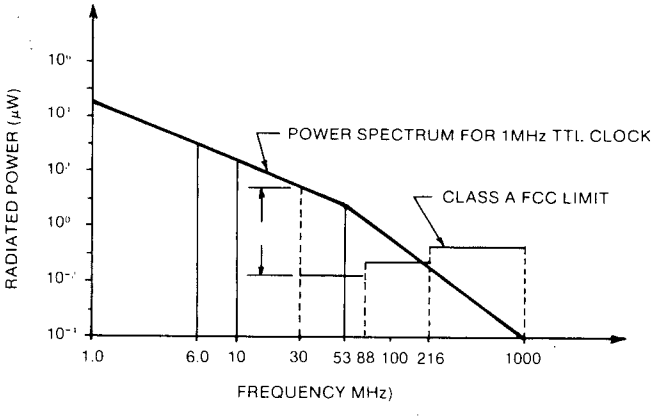

Figure 2. Emission Levels. Shown are both energy available from 1 MHz TTL gate and emission levels allowed by FCC specifications. Graph compares radiation available to that of theoretical isotropic radiator emitting energy equally in all directions at FCC limits.[1]

of the power available in a single TTL gate could result in a violation.[1] (See Figure 2.)

Careful selection of bypass capacitors at all system levels will help minimize RF emissions. High value bypass capacitors (50 μF–100 μF) should be used at the system level, median values (0.47 μF–1 μF) at the board level, and low values (0.01 μF–.1 μF) at the circuit level. By design, high frequency noise should be confined to the smallest loops possible to minimize radiation and all capacitors should have as broad a frequency response as possible for their value. Where large value electrolytics or tantalums are required, they should be bypassed with smaller ceramic capacitors to take advantage of their high frequency performance.

Shielding the equipment enclosure effectively reduces radiation, but any opening, such as cooling slots, I/O ports, etc., can be a major source of RF leakage. Conducted emissions can travel from the digital circuits through the power supply and out through the AC cord. The AC line cord can also act as a receiving antenna for emissions from other parts of the equipment. Correct power line filters are a must to meet the FCC regulation with most equipment.[2]

However, the largest source of radiated emissions is from the I/O cables.[3] Since the attached I/O cables are long wires, they are very efficient radiators below 100 MHz. Even with shielded cables, the elimination of RF frequencies through filtered connectors is required in most equipment. Discoidal MLC capacitor arrays provide a means of obtaining effective connector filtering at a low cost and with improved reliability. Discoidal arrays are specifically designed for filtering out EMI emissions within the connector. They are available in a variety of electrical and physical configurations to match the pin placement of all popular connectors. Their precise construction allows for ease of assembly inside the connector shell. In addition, their multilayer ceramic (MLC) configuration offers a large range of capacitance values for a wide range of attenuation.

MECHANICAL CONSTRUCTION

The design and construction of single and multiple multilayer ceramic capacitors are covered in several technical papers.[3,4] Basically, it is the stacking of ceramic sheets containing two sets of offset, interleaved planar electrodes into a monolithic block. (See Figure 3.) By correctly locating metalized holes in the ceramic discoidal type feed-thrus, capacitors can be con-

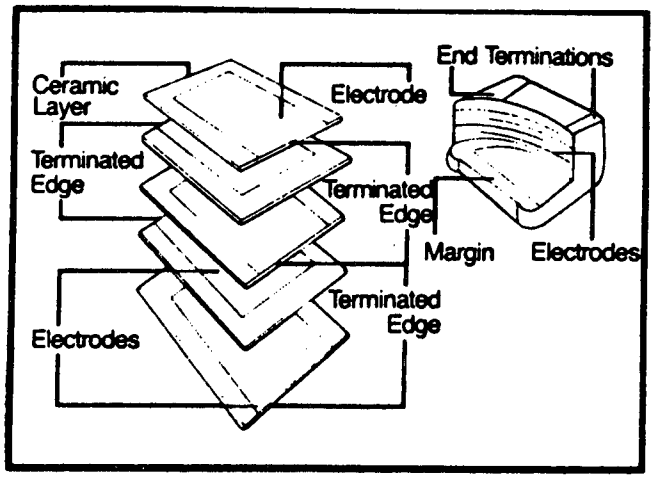

Figure 3. Construction of a Multilayer Ceramic Capacitor.

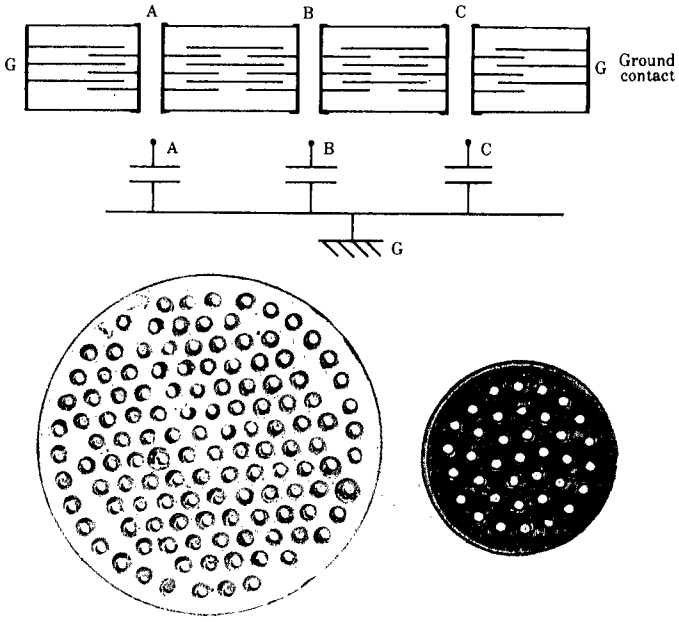

Figure 4. Construction and Schematic for Discoidal MLC's.

structed as shown in Figure 4. The electrodes contacted by the feed-thru form a capacitor to ground through the counter electrode. A common ground connection is normally terminated along the long edges of rectangular arrays and around the periphery of circular arrays. The ground can also be brought to the pin(s), but an edge ground is preferred for solid RF performance. Contact can be made by soldering to a standard silver-palladium termination, a technique well proven with MLC chips.

Discoidal arrays can be manufactured in a variety of sizes and configurations. Table 1 outlines the range of the dimensions and tolerances available. Tooling costs and turn-around times are reasonable. Standard configurations are available for the more popular connector styles and these are listed in Table 2, along with their standard electrical ratings.

Size: Max 2" × 2" (50.8 × 50.8mm); Min .04" × .05" (1.20 × 1.27mm)
Tolerance ± .006" (± .152mm)
Thickness: Max .118" (3.00mm); Min .03" (.762mm); Tol .003" (.076mm)
Camber: .004"/" (mm/mm)
Hole Size: Max .07" (1.78mm); Min .02" (0.5mm); Tol ± .002" (.05mm)
Hole Center: ± .003" (± .076mm)
Termination Materials: Ag, Ag Pd, Au, Au Pt, various platings, barrier layer

Table 1. General Mechanical Specifications.

Rectangular Sub-Miniature D Array Dimensions - inches (mm)

	Length	Width
9 way	.565 ± .007 (14.35 ± .18)	.361 ± .004 (9.17 ± .10)
15 way	.889 ± .007 (22.58 ± .18)	.361 ± .004 (9.17 ± .10)
25 way	1.437 ± .007 (36.50 ± .18)	.361 ± .004 (9.17 ± .10)
37 way	2.085 ± .011 (52.96 ± .28)	.361 ± .004 (9.17 ± .10)
50 way	1.869 ± .013 (47.47 ± .33)	.468 ± .003 (11.89 ± .08)

Normal hole diameter	.0465 ± .0025 (1.18 ± .07)
Normal array thickness (for capacitance/ contact up to 20nF	.060 ± .005 (1.52 ± .13)
Array thickness for capacitance/ contact up to 30 nF	.090 (2.29)
(For higher capacitance values please inquire)	
Standard capacitance values	0 - 5nF
Standard capacitance tolerance	± 20% or GMV (Guaranteed Minimum Value)
Working voltage	50v, 100v, 200v
DWV in air	500v

MIL-C-26482 and MIL-C-38999 Circular Array Dimensions - inches (mm)

	Array Diameter	Hole Diameter
19 way	.727 ± .005 (18.47 ± .13)	.046 ± .003 (1.17 ± .08)
26 way	.857 ± .005 (21.77 ± .13)	.046 ± .003 (1.17 ± .08)
32 way	.897 ± .005 (22.78 ± .13)	.046 ± .003 (1.17 ± .08)
37 way	.665 ± .005 (16.89 ± .13)	.036 ± .003 (.91 ± .08)
41 way	1.004 ± .005 (25.50 ± .13)	.046 ± .003 (1.17 ± .08)
61 way	1.242 ± .005 (31.55 ± .13)	.046 ± .003 (1.17 ± .08)
128 way	1.242 ± .005 (31.55 ± .13)	.036 ± .003 (.91 ± .08)

Normal array thickness (for capacitance/contact up to 5nF)	.040 ± .005 (1.02 ± .13)
Array thickness for capacitance/ contact up to 10nF	.090 (2.29)
(For higher capacitance values please inquire)	
Standard capacitance tolerance	± 20% or GMV (Guaranteed Minimum Value)
Working voltage	50v, 100v, 200v
DWV in air	500v

Table 2. Array Dimensions.

CERAMIC MATERIALS

Discoidal arrays are manufactured in all three standard MLC dielectrics: NPO, X7R, and Z5U, thus offering a wide range of capacitance values at various levels of stability. The properties of these three materials are summarized in Table 3. Their capacitance changes with temperature are plotted in Figure 5.

For the military temperature range, X7R (BX) is usually recommended. In the limited temperature range for most commercial applications, the high "K" of Z5U dielectrics can be used to obtain lower costs.

The resistivity of the buried electrode and interconnections can be varied between 50–350 MΩ per square. Actual resistance is lower since there are usually many layers (up to 100) interconnected to form the capacitor electrodes.

Properties	NPO	X7R	Z5U
Volume resistivity greater than	.....	5×10^{12} ...	.....
Dielectric constant	70	2200	9000
Thermal Expansion Coefficient (inch (mm)/inch (mm)/°C)	10.5×10^{-6}	12.0×10^{-6}	11.5×10^{-6}
Thermal Conductivity (25°C, W/M²/K°)	.....	4 - 5	.....
Capacitance per cubic inch, μF	13	222	578
Capacitance per cm³, μF	0.793	13.5	35.3
The above figures are for 50v DC working; the capacitance per cube can be considered to be approximately inversely proportional to the WVDC.			
Cap Tolerance % (without adjustment or special electrode design)	10	20	20
DF %(1 KHz), 25°C	.15 max	2.5 max	3.0 max
Typical TC Tracking %	0.1	1	10
Cross-Talk Max pF	1	3	3
WVDC Max 500, Min 50			

Table 3. Dielectric Materials.

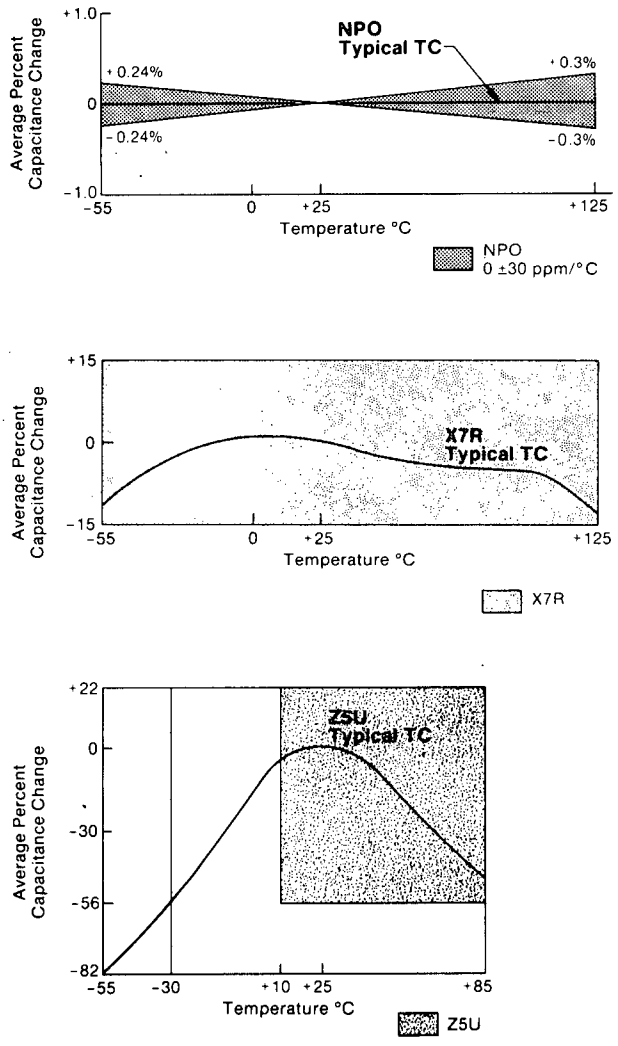

Figure 5. Typical Temperature Coefficient Curves.

ELECTRICAL PERFORMANCE

The discoidal capacitor arrays are usually assembled into "π" or "C" filters inside the connector by their manufacturer. This insures sharper cut-offs and some higher band attenuation. (See Figure 6.)

The desired insertion loss change with frequency can be obtained by selecting the required capacitance value from the curves in Figure 7. These curves are based on a single discoidal capacitor with no ferrite beads added and assume a good ground plane. As can be seen, the measured values compared closely with the calculated values.

The insertion loss for a standard D-Subconnector array with a nominal capacitance value of 875 pF per

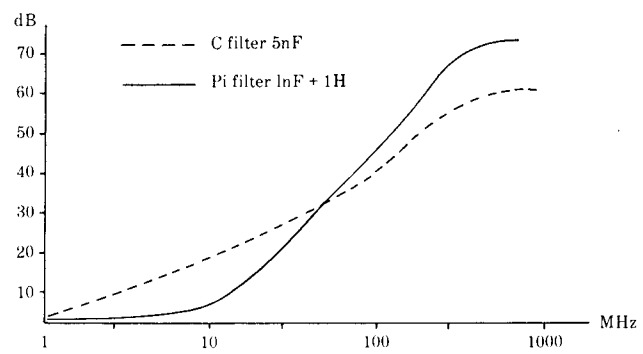

Figure 6. Typical Insertion Loss Characteristics (MIL-STD-220).

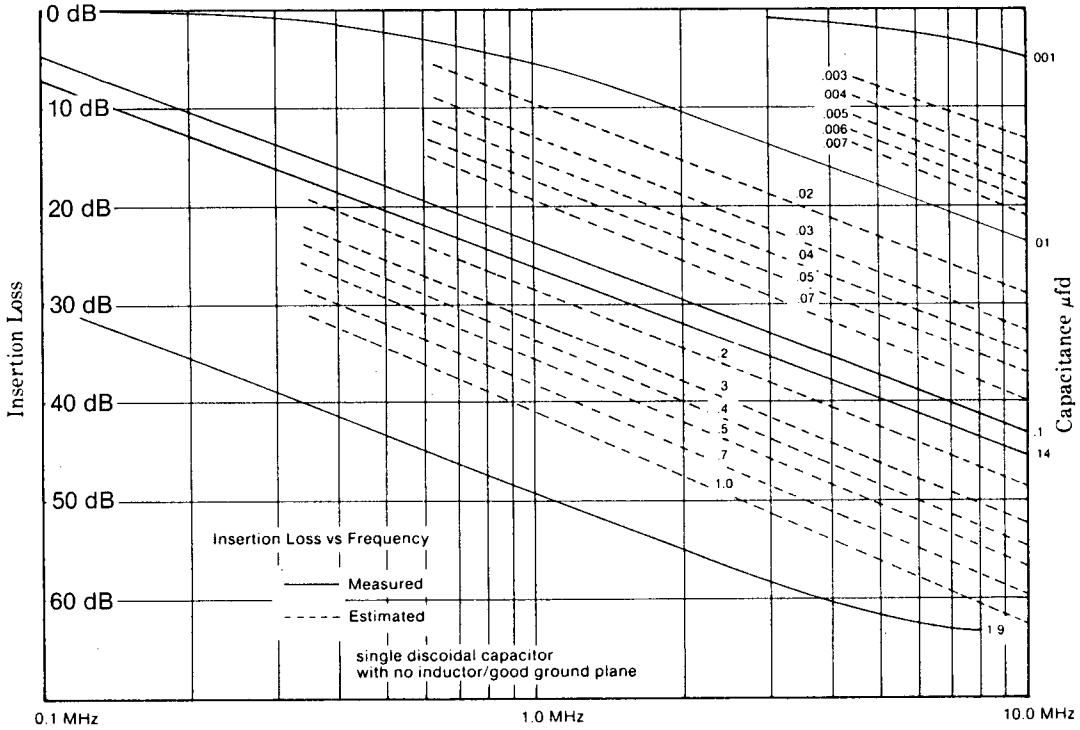

Figure 7. Insertion Loss vs Frequency.

hole is shown in Figure 8. The three scans show similar attenuation regardless of the hole location in the array. Figure 9 shows the insertion loss on the same array with a small ferrite bead added having approximately 0.7 nh inductance.

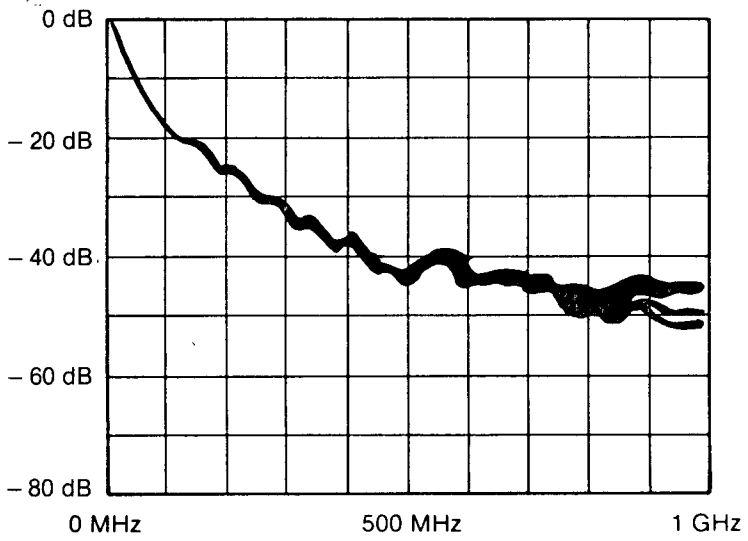

Figure 8. D-Sub connector with 875 pfd/hole Capacitor Array. Scan of 3 separate holes (center top row, center bottom row, and end corner hole).

The insertion loss of a standard 19-hole array with 5,000 pF per hole capacitance is shown in Figure 10. Figures 11A and B indicate the improvement gained when a small ferrite bead is added. The sharper cut-off is particularly noticeable at the lower frequencies, but some additional attenuation is gained at higher frequencies.

Even with the higher "K" materials used in the arrays, good separation of the input signal is maintained. The "cross-talk" between various holes of the 19-hole array with 5,000 pF capacitance per hole were monitored by the test set-up in Figure 12. Greater than 80 dB separation was maintained between adjacent holes to 100 MHz. (See Figure 13.)

DISCUSSION

Discoidal array capacitors assembled into connectors effectively bypass high frequency noise to ground before it can be radiated from I/O cables. Although the amount of attenuation required to meet the FCC regulation varies according to the equipment under test, most discoidal capacitance values show insertion losses greater than 20 dB (usually considered an acceptable level for low-pass filters) from less than 10 MHz to 1 GHz. The multicapacitor construction insures that each pin in the connector is filtered. It also reduces the number of interconnections, and thus cost, of the assembly over individual discrete tubular capaci-

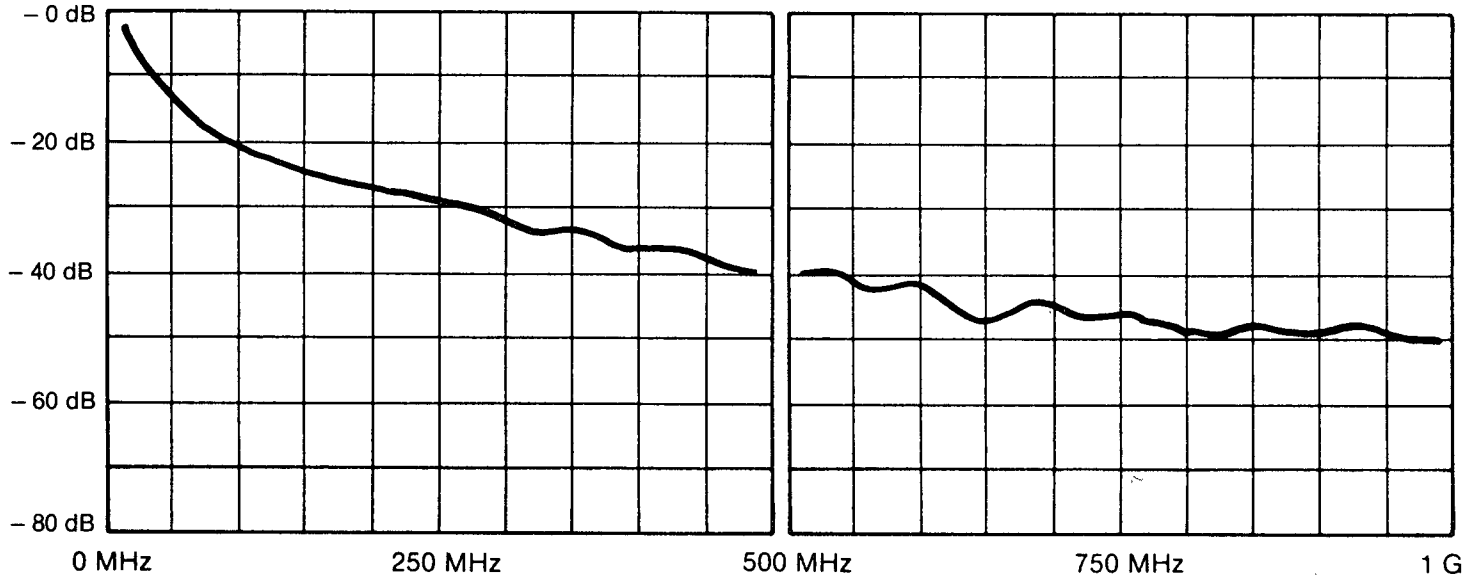

Figure 9. D-Sub connector (same as in Figure 8) with Small Ferrite Bead (0.7nh) Added.

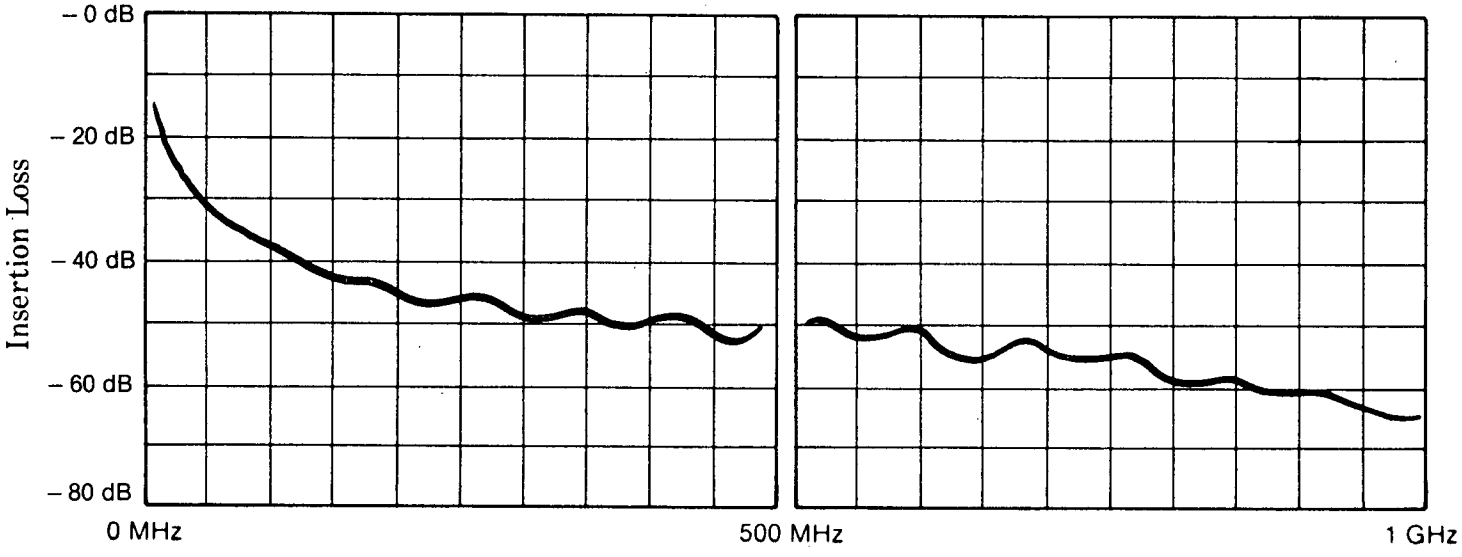

Figure 10. 19 Hole Array with 5000 pfd/hole Capacitance to Ground.

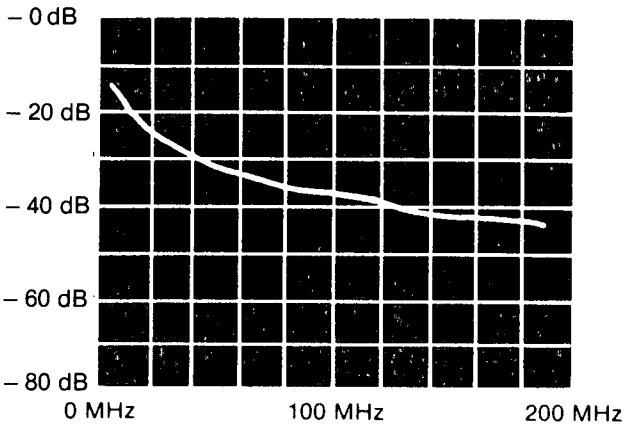

Figure 11A. Single Hole in 19-hole Array with 5000 pfd/hole and No Ferrite Added.

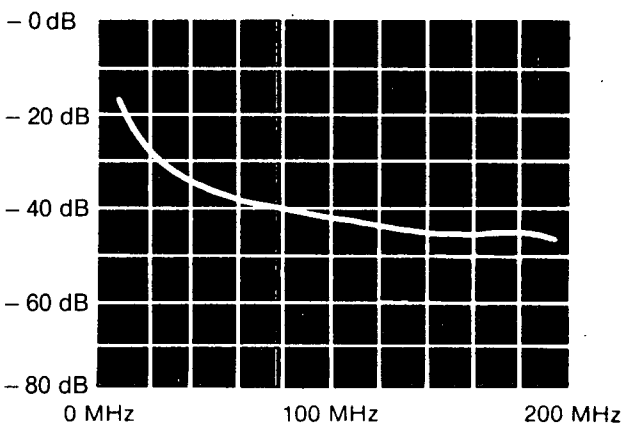

Figure 11B. Same Hole as Above Array with Small Ferrite Bead Added.

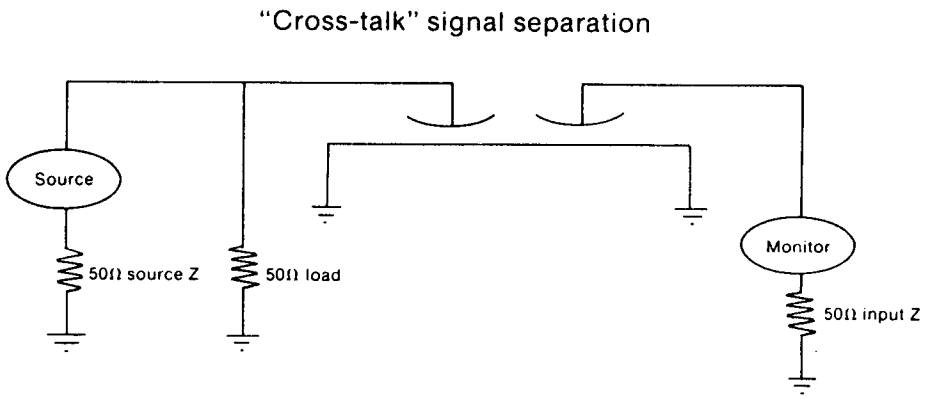

Figure 12. Test Setup for Measuring "Cross-talk."

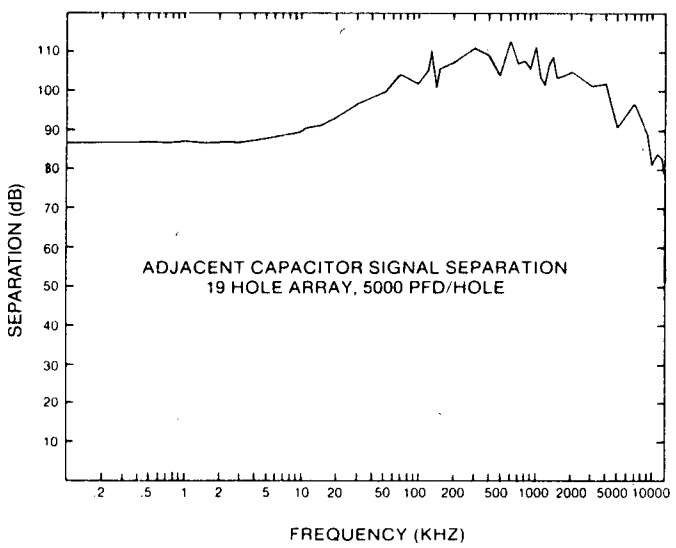

Figure 13. Adjacent Capacitor Signal Separation, 19-hole array, 5000 pfd/hole.

tors attached to each pin. This construction improves yields on interconnections alone by over 50%.

Discoidal arrays have been tested by the military for use in protected header assemblies and found to exhibit very good loss characteristics with particularly impressive high loss values from 1 to 10 MHz.

REFERENCES

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