MLC CAPACITORS IN EMI/RFI APPLICATIONS

The use of a low-pass filter can often solve a high-frequency problem. Form flexibility is a major advantage of MLC capacitors and results in reduced labor and rework, increased reliability and performance consistency.

John Prymak and Sharan Narula, Olean Advanced Products, Olean, NY

INTRODUCTION

One of the simplest solutions to a high-frequency problem is the use of a low-pass filter. A capacitor in parallel with the load or transmission path exhibits decreasing impedance as frequency increases. This shunting effect can be increased with the addition of an inductance in series with the load, which makes the impedance at the load or transmission path appear higher as frequency increases. The low-pass circuit is so simple to understand and so easy to implement, it is sometimes forgotten that ideal component calculations must be adjusted to real world component uses. Unless the high-frequency performance of the capacitor and the connection circuitry is taken into consideration, the problem might appear unsolvable.

LOW-PASS FILTER

The ideal capacitor has no inductance and no resistance. Its impedance is its capacitive reactance only. In an ideal 50-ohm system, the insertion loss can be calculated using Equation 1. This is the ratio of signal into a perfect 50-ohm load with a capacitor shunting the signal to that of the perfect 50-ohm load with no shunting device. The rate of loss increase calculates to approximately 6 dB per octave or approximately 20 dB per decade.

If the problem is at specific frequencies, the cap for achieving the desired loss at each problem frequency can be calculated using Equation 2. The largest cap from all the calculations would then be chosen. Additional consideration must be given to the cutoff frequency of the chosen capacitance. The cutoff frequency must be high enough so as not to interfere with required signals (Equation 3). This cutoff frequency is the one where the impedance of the capacitor equals that of the load.

$$dB = -10 \times \text{Log}_{10}[(50 \times \text{Pi} \times \text{Freq.} \times \text{Cap})^2 + 1] \quad (1)$$

$$C = [10^{dB/10} - 1]_{1/2}/(50 \times \text{Pi} \times \text{Freq.}) \quad (2)$$

$$\text{Freq.}_{(-3dB)} = 1/(2 \times \text{Pi} \times \text{Cap} \times 50) \quad (3)$$

The choice of a capacitor must be based on its task. It must have high-frequency capabilities, but this requirement does not immediately dictate that it be constructed of materials which provide the highest possible Q. The Q, or Dissipation Factor, (DF – inverse of Q) is usually measured at 1 kHz - hardly the frequency where the desired effects are needed. Its impedance at the higher frequencies is the major consideration. Although it might not be readily recognized, the ability of a high lossy dielectric in a bypass application can match that of a high Q-type ceramic of equal capacitance. To be exact, its impedance relative to the load or transmission impedance is the most important consideration. The low-pass circuit with capacitor is a shunting circuit, and how well the shunt passes the high frequencies is the measure of its real capabilities.

THE MLC SOLUTION

One of the advantages of the ceramic MLC (Multi-Layer Ceramic) capacitor lies in its form flexibility. It can be built in almost any shape or configuration. A discoidal MLC is built to fit within a coaxial signal line, giving extremely good high-frequency capabilities. This capacitor, as depicted in Figure 1, has a very low inductance since the signal path through the capacitor emanates from the center conductor to the outside shield outward 360 degrees. Its behavior in application duplicates the projected ideal up to an insertion loss of approximately 70 dB. In analyzing the performance of this type unit with that of a surface mounted chip, the insertion loss must be considered. Figure 2 shows the discoidal capacitor with its 6 dB per octave loss, and the chip with its steep loss dependance which then returns to a constant loss at about 20 dB. With the surface mounted chip, a unidirectional signal path is dictated by its structure. There are also constraints at the points of attachment to the signal line and to the ground. These conditions require the addition inductances over those of the discoidal. (These constraints of attachment would be increased considerably if the chip were replaced with a leaded device.)

The chip capacitor has a higher inductance. Before the self-resonance of the chip is reached, the capacitive reactance is opposed by the resultant inductive reactance. The vector sum is lower, though still capacitive, giving the appearance that the magnitude of the chip capacitor is increasing. The impedance is inversely proportional to both capacitance and frequency; and the net result is that the insertion loss increases at a rate much greater than projected in the early stages, at least, until self-resonance is reached and the inductive element dominates. At that point the insertion loss decays to

a point where increases in frequency do not change the ratio of signals through the capacitor and the load.

As an additional note of interest, two surface-mounted chips of identical geometry with one constructed of NPO and the other of X7R, were tested for insertion loss. The insertion loss for each chip was similar to the response of the chip shown in Figure 2. Although they showed different frequencies of maximum insertion loss because of their different values (800 and 1800 pFd), they both leveled off at approximately the 20 dB level.

In Figure 3, the impedance and ESR (Effective Series Resistance) for two connectors are shown.The unit exhibiting higher self-resonance (86 MHz) is a discoidal type while the other is an MLC chip (44 MHz). The insertion loss data of these units is shown in Figure 2. The difference in inductance which causes this shift is approximately 11.4 nH (15.9 nH chip versus 4.5 nH discoidal). This difference is not significant unless it is analyzed in terms of the chip being 240 percent higher than the discoidal.

These values are not typical of the component itself but represent the sum of component and leads, plus any added parasitics from the shell. The actual inductance measured from the chip outside of the container is 1.5 nH, with an apparent self-resonance of 150 MHz.

MULTIPLE LINE CONNECTORS

As previously mentioned, the form factor of the MLC device is very important. Because its shape can be varied and its multilayer and plate screening methods allow so much freedom, a collection or array of capacitors can be manufactured within a singular element. In many cases, these elements are individual discoidal capacitors where multiple

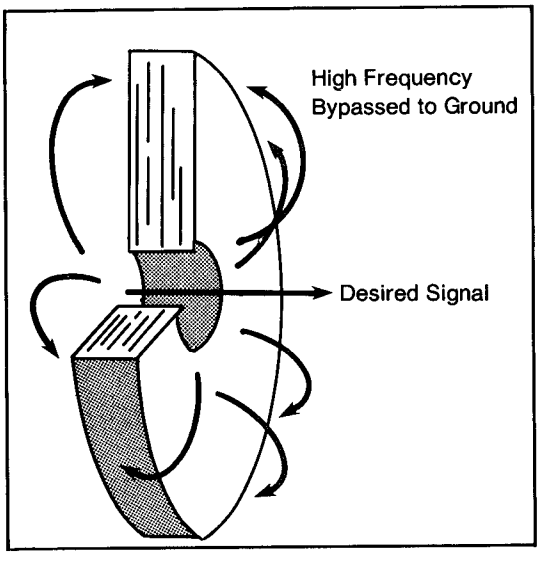

Figure 1. Discoidal Capacitor.

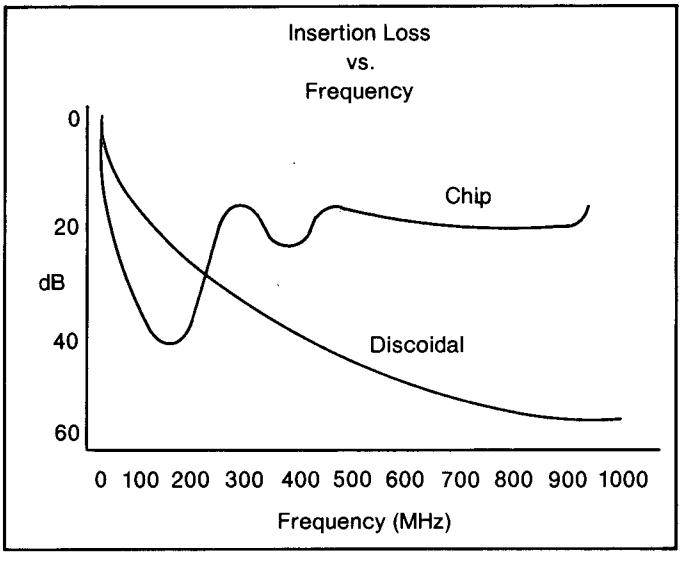

Figure 2. C ~875 pFd Discoidal Versus Chip.

holes are drilled within a larger plane. The larger plane's shape is determined by the shell through which the multiple signals pass. The overall shape of the planar array is usually circular or rectangular. Odd shapes for fitting radial trapezoids (D-Subminiature) or circular configurations with multiple circular notches have also been manufactured.

Figure 4 shows a typical discoidal array arrangement. Where each pin connects to a hole, circular plates extend into the body of ceramic for a short distance. These plates are connected only to the one hole. Multiple ground plates extend throughout the shape of the array except where the holes exist. A margin of separation is maintained to ensure that the ground electrode plate does not come near the hole walls. There is an overlap area where the ground plates extend into the regions of the plates attached to the holes, and this area is where the capacitance is concentrated. As with earlier MLC devices, controlling the overlap areas and dielectric thickness allows control of capacitance. Maintaining margin integrity ensures reliability equal to single chips.

What are the benefits of a single array versus multiple capacitors on all pins? Labor costs and rework are immediately reduced because all the devices are inserted in a single step. Reliability is increased because rework, for the benefit of one pin and to the possible detriment of other pins, has been eliminated. All the pins connected to capacitors are processed at the exact same time and are of the exact same material. The temperature and environmental characteristics are the same for all pins because the material and processes are, again, exactly the same.

The available capacitive arrays are quite numerous. The largest *standard* array contains 128 pins (capacitors) in a 1.242-inch diameter circular plane, 0.100-inch thick. The largest *standard* rectangular array contains 50 pins (capacitors) in a 1.873 x 0.468 x 0.100 package. There are also *standard* designs with varied hole radiuses and capacitance within a singular element. Table 1 gives mechanical and physical properties of the arrays and materials.

PERFORMANCE REQUIREMENTS

For military applications, perfor-

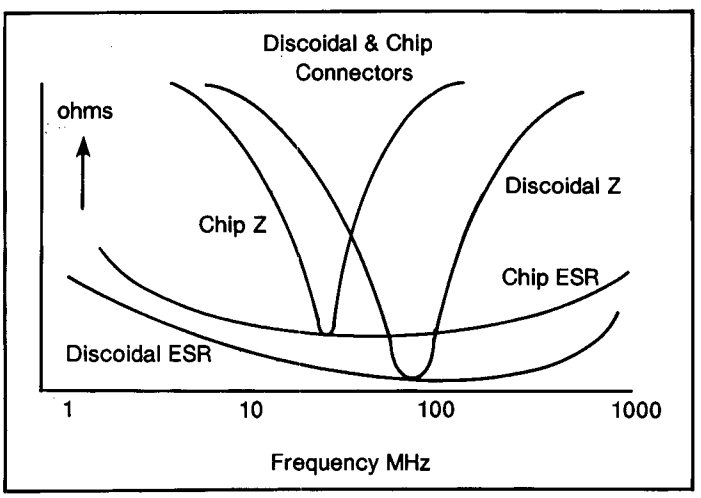

Figure 3. Impedance and ESR Versus Frequency.

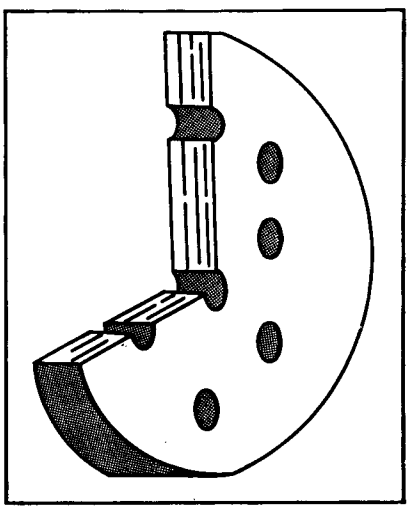

Figure 4. Discoidal Planar Array.

ARRAY/SUBSTRATE DESIGN GUIDELINES	
Max. Size	3" x 2" (± .5% Tol) x 0.120"
Min. Hole Size	0.020" (± .003" Tol)
Max. Hole Size	0.180" (± .003" Tol)
Min. Hole Separation	0.040"
Min. Edge Termination Band	0.020"
Edge Termination Material	Fritted Ag (Substrate) Plated Ni/Au (Array)
Max. Capacitance/Area (sq.in.)	1.3 Mfd (NPO) 22 Mfd (X7R) 58 Mfd (Z5U)
Max. Designed Cap Range	2 orders of magnitude
Flatness	0.004"/linear inch
CTE (ppm/°C)	10.5 (NPO) 12.0 (X7R) 11.5 (Z5U)

Table 1. Array/Substrate Design Guidelines.

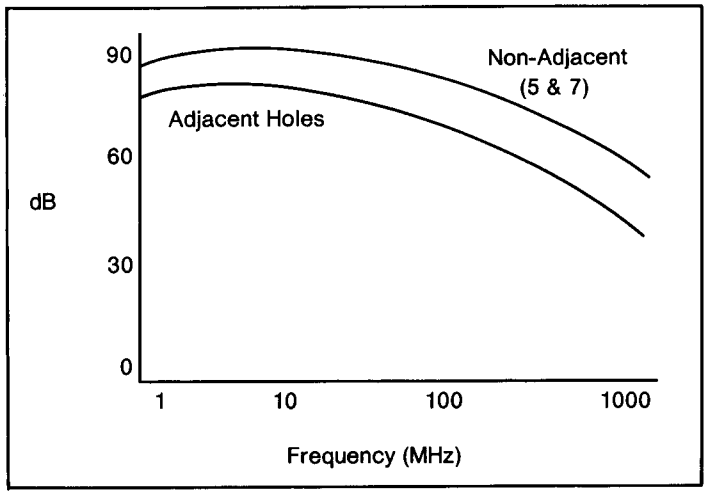

Figure 5. Cross-talk 25-Pin D-Sub Filtered Connector.

mance of the discoidal capacitor or planar array is essential. For many other applications, the violation of FCC-mandated limits on EMI/RFI (Part 15, Subpart J) must be by less than 30 dB. Because the source and load impedances might be as much as 600 ohms, the performance of the chip may be more than sufficient. The cost for this type connector is significantly lower than a discoidal array.

For telecommunication signal processing, there is an additional requirement of 1000 Vac temporary overload capacity (FCC Part 68.302). Chips small enough to fit the pin-dictated nests rarely meet this requirement. An alternative to the chip would be window arrays. These are MLC arrays with metal strips exposed to make spring-pressed contact with pins parallel to the plane of the array. The cost per line on connectors utilizing more than 24 pins can be as low as $0.04. The windows are on both sides of the array allowing two rows of pins to make contact to a single array set between them.

The insertion loss of this device is essentially the same as the single chip with one important exception; this array successfully passes the 1000 Vac test. Typical dc breakdown is well over 2000 Vdc. There is an 8 to 10 dB difference between center pad (window) and outside pads. This difference occurs because the ground termination plate is terminated only at the outside edges and because the impedance for the center signal path is slightly higher than that of the outside pad.

CROSS-TALK CONSIDERATIONS

Since the entire package is built within the dielectric, signal transfer from one hole is dependent on the following factors: hole density, dielectric constant, number of electrode layers, distance between plate edges, and ground termination. The distance between adjacent holes is inversely proportional to the stray capacitance; the dielectric constant is directly proportional to this capacitive coupling between these holes. The number of edges extending from each hole also adds to the coupling capacitance. This coupling impedance is in series with the adjacent hole capacitance; together they are parallel with the load and the signal (or source) pin capacitance to ground.

Figure 5 displays a typical cross-talk measurement for adjacent pins in a 25-pin D-Sub array. The material is X7R with a capacitance of 1000 pFd per hole. The measured stray capacitance is approximately 30 pFd (ground is tied to a guard circuit at 1 kHz).

If the impedance of the ground plate is kept to a minimum, the cross-talk separation would be maintained at high levels. If the ground plate impedance is effected by poor connection or thinner materialization, the effective resistance and inductance would increase to the point where separation would be minimal. The cross-talk results shown are taken from an assembled connector with soldered ground connections along the longest edges only and with chassis connection through two mechanical screwed connections. The results could be improved by utilizing full perimeter solder connection and full perimeter contact of the shell to the chassis. ■

BIBLIOGRAPHY

Hazzard and Prymak, "EMI Suppression Utilizing MLC Discoidal Arrays," ITEM 1985.

Hazzard and Kiefer, "EMI Reductions Using Capacitive Filter Connections," AVX Technical Paper.

Martin and Keenan, "Improved Noise Suppression Via Multilayer Ceramic Capacitors (MLCs) in Power Entry Decoupling," AVX Technical Paper.