Implications of decreasing circuit card trace size and spacing in a lightning environment

Lightning protection devices and other inherent design parameters can cause common-mode lightning-induced voltages to appear as potential differences between neighboring circuit card traces.

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Circuit card designs are moving toward saving costs and size by reducing circuit card dimensions. This dimension reduction is accomplished by reducing trace width and spacing between the lines on circuit cards. The idea of trace lines with smaller dimensions and finer spacing is gaining more attention since it reduces the total circuit card area and limits the number of layers. These savings ultimately result in a cost reduction for producing circuit cards.

The broad range of possible applications for small circuit cards includes many critical areas. A few examples of critical applications are: military equipment performing critical functions; equipment used for the exploration of space; and avionics equipment where the safety of flight depends on properly functioning critical equipment.

The smaller trace dimension and finer spacing in circuit cards will be primarily designed to carry electrical source voltages limited to a maximum of 33 V, with signal voltages not exceeding 3 to 15 V, and trace currents limited to a few amperes. Special attention and consideration to the circuit card design will be necessary to ensure the ability of the card circuits to perform their functional operations in adverse environments. There are many environments in which the circuit cards have been employed to perform critical category functional operations.

One of these areas is high altitudes, where the lower dielectric strength may increase the probability of inter-trace dielectric breakdown in the circuit cards. In the lightning environment, which may exist at both ground level and in the inter-cloud spaces at higher elevations, high voltages which are induced in equipment cable wiring and carried to the circuit card traces are considered the main causes of sparkover between the traces. These sparkovers may contribute to the inter-trace electro-migration in the circuit card dielectric medium.[1] High relative humidity, smog, dust, and other pollution in the air surrounding circuit cards can easily increase the chance of breakdown, facilitate the triggering of inter-trace and trace-to-ground sparkover, and contribute to worsening effects of electro-migration.[1,2] This would result in component damage and shortening of the circuit card mean time between failures (MTBF).

In particular, the circuit cards used in avionics equipment that operates in high

altitudes and is exposed more often to lightning environments should be designed such that no adverse effects on the circuit card electronic components and operational functions are produced by the lightning environment.

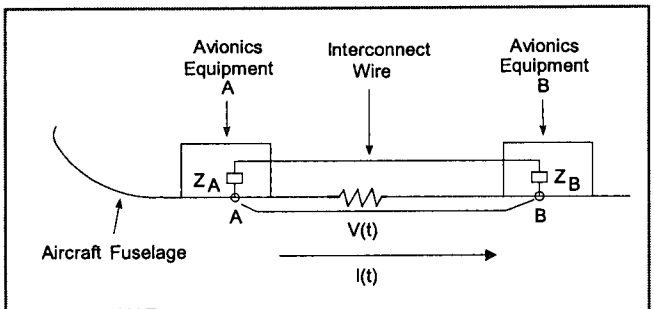
LIGHTNING ENVIRONMENT INDUCED TRANSIENT WAVEFORMS AND PEAK AMPLITUDES

Electronic equipment operating in lightning environments must be hardened against lightning-induced transients. Hardening is necessary to insure that components on the equipment circuit cards remain immune from damage and the equipment operational functions are protected from upset. A good example of such equipment is shown in Figure 1. The avionic equipment is installed in an aircraft at locations A and B with the aircraft fuselage used as a ground.

Experimental observations of transients recorded when the aircraft is struck by lightning indicate that transient voltages resulting from potential differences between points on the fuselage, magnetic field coupling, and those resulting from fuselage/cabling electrical oscillations, have waveforms which can be approximated by the waveforms in Figures 2, 3, 4, and 5 for the various levels of the lightning category.[3,4]

LIGHTNING PROTECTION, INTERFACE HARDENING CONCEPT AND DEVICES

Interconnect wiring loops are formed when the cable wiring entering the equipment cable receptacle terminates on the circuit card interface traces which are connected to the circuit card impedances of electronic and electrical components. The lightning-induced voltage waveforms described in the previous section then become the loop driving source which injects the lightning currents into the circuit card through the interface trace impedance (Figure 6). Protection of sensitive cir-



V(t) = I(t)R
V(t) = Induced voltage surge
I(t) = Lightning current passing through fuselage
Z_A, Z_B = Equipment input pin impedance which includes fuselage grounding straps
R = Fuselage resistance

Figure 1. Using the fuselage as a ground plane in avionics installations.

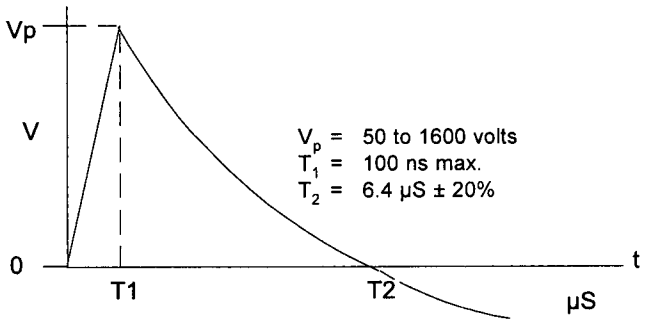


Figure 2. Voltage waveform.

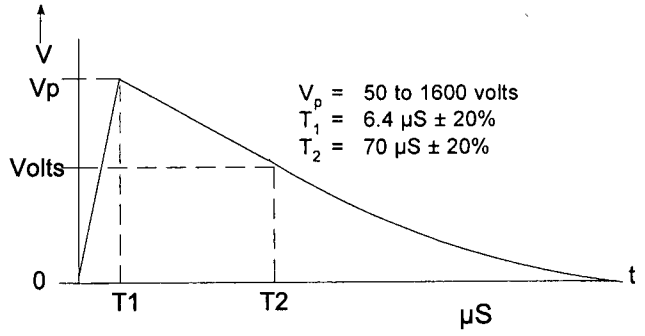


Figure 3. Voltage Waveform 4.

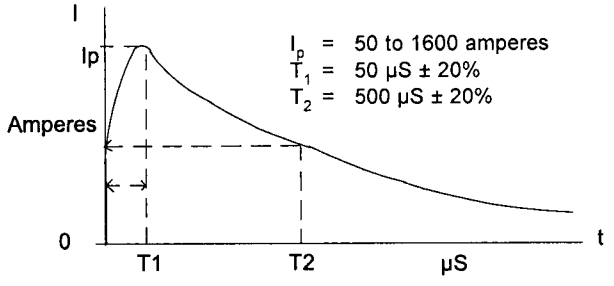
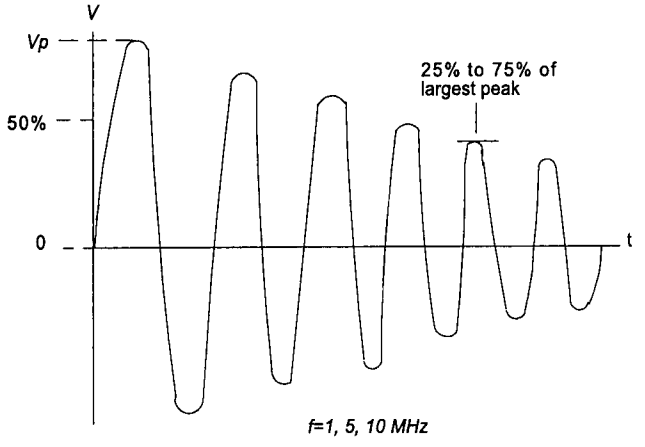


Figure 4. Current Waveform 5B.



V_p = 100 V to 3200 V

Figure 5. Voltage Waveform 3.

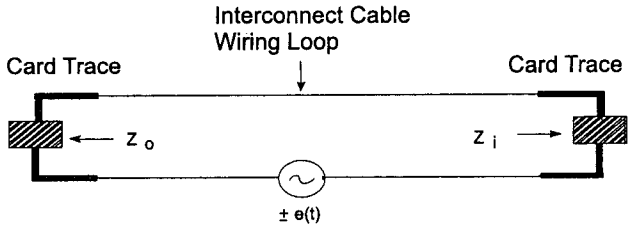


Figure 6. Prior to protection of interface pins, z_i and z_o are the pin input and output impedances comprised of resistive and reactive circuit elements measured between the pins and equipment chassis.

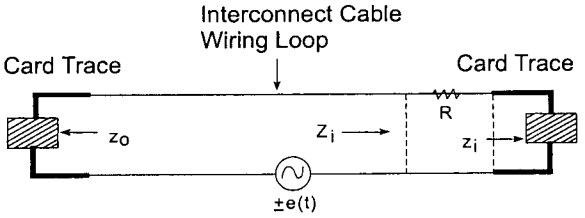


Figure 8. Lightning protection component R imposes a new input impedance Z_i = R.

cuit components from the adverse effects of the lightning can be accomplished by clamping the lightning-induced voltages at the trace input or by limiting the lightning current in the wiring loop in order to prevent the lightning energy from reaching the circuit card. In Figure 7, the Transorb® D (which limits the lightning voltage, and diverts and absorbs a large portion of the lightning current away from entering the circuit card), and in Figure 8, the large resistor R (a 10- to 24-kW, 1/8-watt resistor to limit the lightning current below the damage level of the interface components), are examples of modern lightning protection design techniques and devices.[5]

As shown in Figure 7, the Transorb® imposes a new impedance at the circuit card trace when lightning strikes. In the case of the protective device such as Transorb® D, impedance z_i is replaced by Z_i which is equal to the Transorb® forward impedance (usually a small resistance equal to r_f = 0.1 ohm << $|z_i|$) for the negatively induced lightning pulse. When the lightning-induced voltage in Figure 7 is positive, the Transorb® input voltage is clamped at $V_i = i_b \bullet (r_b + V_{BD})$, where r_b is the reverse breakdown resistance and V_{BD} is the device breakdown voltage. The input impedance Z_i then becomes equal to r_b (which for Transorbs® is equal to 0.5 ohm and also much smaller than $|z_i|$). In the case of series R>>$|z_i|$ added as a protection component in Figure 8, z_i is replaced by Z_i = R as the new trace impedance imposed by the protective component R.

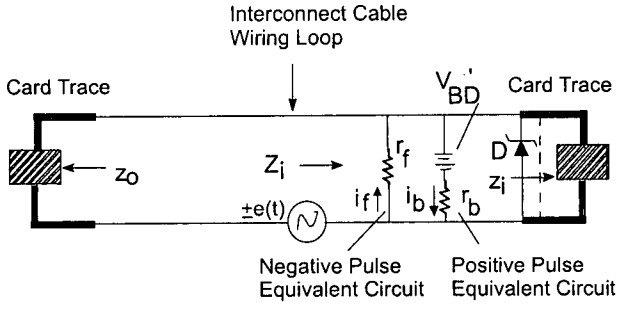


Figure 7. Lightning protection device D imposes a new input impedance $Z_i = r_f$ for negative and $Z_i = r_b$ for positive lightning pulses.

STATE-OF-THE-ART CIRCUIT CARD DESIGN WITH 12-MIL TRACE LINE SPACING

For moderate lightning environments defined as Level 3 in RTCA document DO-160[3], the 12-mil circuit card line spacing is sufficient to circumvent spark triggering and inhibit arcing in the inter-trace spacing, in the dielectric medium, and spaces between traces and the layers of ground planes. Twelve-mil spacing immunity from circuit card sparkover and arcing implies that the lightning-induced voltages shall be confined to 300-V and 600-V ranges for double exponential waveform and the damped sinusoidal waveform respectively. In circuit boards for which the EMI design guidelines have been fully implemented, only the interface circuits must be hardened whenever damage and upset prevention for a typical equipment functioning in the lightning environment is desired or required. Then, in the absence of inter-trace sparking and insulation breakdown of the substrate layers, both isolated and buried circuits will remain immune from the effect of immediate damage and failures caused by lightning.

Following state-of-the-art design hardening techniques against lightning, and adhering to the lightning protection design guidelines, devices such as Transorbs® can be deployed to limit the lightning voltage and absorb the lightning energy (Figure 7). The use of Transorbs® as lightning protection devices becomes mandatory when the total impedance of the loops terminating on interface pins can not be increased to limit the lightning current, or the lightning energy can not be diverted by using passive low shunt impedances at the interface pins.

However, because of the higher component and maintenance cost for Transorbs®, higher priority and preference is given to the addition of passive shunt elements at interface pins, or passive series components in the interface circuit loops (Figure 8), in order to reduce and limit the effects of lightning.

REDUCTION IN TRACE SPACING

It has been observed that cost-saving trends are directed to reducing the circuit board size (area and the number of board layers). This, in turn, mandates the use of smaller circuit board spacing in order to accommodate the same number of electronic circuits and components on the circuit cards. As the distance between trace lines and

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ground planes/traces decreases, the possibility of sparks and arcing in the inter-line spacings and the chances of breakdown in the board substrates increase. The main concerns are arcing between the circuit board traces and breakdown in the insulation substrates that could be detrimental to components and circuit boards used in electronic equipment circuit cards.

In the analyses and discussions that follow, it will be assumed that, in pursuit of new trends in circuit board technology, the line spacing and the inter-layer substrate thickness have decreased such that the threat of inter-trace arcing and inter-substrate breakdown exists. Since using circuit boards crowded with smaller line spacings will find extensive application in the foreseeable future, the ultimate goal is to provide these circuit boards with protection from lightning-induced transients. That is, the objective is to protect the circuit board and the circuit card components from failure and permanent damage, to immunize the functional operations of the circuit cards to upset, and to safeguard the MTBF of the circuit board from degradation.

CIRCUIT BOARD TRACE-INDUCED VOLTAGE THEORY

In general, evaluation of the lightning-induced transient voltages at the circuit board interface traces in avionics equipment may require application of complicated techniques used in coupled mode theory using distributed circuit parameters for traces acting as portions of strip transmission lines. Such is the case when lightning transients, such as short duration Waveform 2 and 10-MHz damped sinusoidal Waveform 3 voltages, are the sources of induced currents in cable wiring with lengths comparable to the wavelength of the frequency content of the transient waveform. However, for induced lightning transients of longer duration such as Waveform 3, 1-MHz damped sinusoidal, or Waveforms 4 and 5 transient pulses, and under conditions of sufficiently small cable wiring lengths and circuit dimensions, the well-established elementary lumped circuit theory can be applied. In order to enhance and demonstrate the existence of large lightning-induced voltages between the traces, the circuit board trace-induced voltage theory is developed for application to typical cable wiring and trace impedance terminations which are specifically selected to confirm the agreement of the experimental results with developed theory based on the well-known lumped circuit theory. For the sake of analysis simplicity, it is assumed that the impedances Z_i and Z_o imposed by lightning are resistive, as are found in most of the circuit card designs (Figure 9).

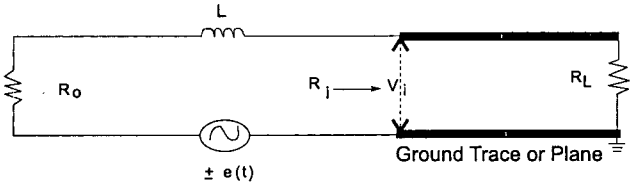

Figure 9. Single interface trace-induced lightning voltage theory.

SINGLE TRACE COMMON-MODE LIGHTNING-INDUCED VOLTAGES

The lightning-induced current flowing into a trace in a single wiring loop is then related to the lightning-induced voltage e(t), the loop self-inductance L, and the input and output impedances R_i and R_o by the well-known lumped circuit equation as follows:

$$e(t) = (R_i + R_o)I(t) + L\frac{d\,I(t)}{dt} \qquad (1)$$

In the case of large terminating input and output impedances $R_i + R_o$, the loop self-inductance termination has insignificant effect on the loop lightning-induced current. In this case, the trace lightning-induced voltage at the trace input with terminating impedance R_i becomes

$$V_i(t) = I(t)R_i = \frac{R_i\, e(t)}{R_i + R_o} \qquad (2)$$

Then for the input loads $R_i << R_o$, the total terminating impedances $R_i + R_o \cong R_o$, and

$$V_i(t) = \frac{R_i\, e(t)}{R_i + R_o} \cong \frac{R_i}{R_o} e(t) \qquad (3)$$

which indicates that the trace voltages are much smaller than the loop lightning induced voltage e(t).

For $R_i >> R_o$, the ratio $\dfrac{R_i}{R_o + R_i} \cong \dfrac{R_i}{R_i} = 1$ and

$$V_i(t) = \frac{R_i\, e(t)}{R_i + R_o} = e(t) \qquad (4)$$

proving that the trace voltage may become as large as the loop lightning-induced voltage. For the special case of $R_i = R_0$,

$$V_i(t) = \frac{R}{R_i + R_o} e(t) = \frac{e(t)}{2} \qquad (5)$$

LIGHTNING-INDUCED VOLTAGES BETWEEN TWO NEIGHBORING TRACES

The dependence of common-mode induced voltages on the loop termination impedances are well understood by considering Equations 2 through 4. The equations for the trace-induced common-mode voltage $e_a(t)$ and $e_b(t)$, and the induced currents $I_a(t)$ and $I_b(t)$ flowing into Traces A and B (Figure 10) due to lightning, can be expressed as

$$e_a(t) = L_a \frac{dI_a(t)}{dt} + I_a(t)R_{ia} + I_a(t)R_{oa} \pm M_{ab} \frac{dI_b}{dt} \quad (6)$$

$$e_b(t) = L_b \frac{dI_b(t)}{dt} + I_b(t)R_{ib} + I_b(t)R_{ob} \pm M_{ab} \frac{dI_a}{dt} \quad (7)$$

where

L_a and L_b = Self-inductance of the cable wiring loops connected to Traces A and B respectively

R_{ia} and R_{oa} = Input and output impedances at Trace A

R_{ib} and R_{ob} = Input and output impedances at Trace B

M_{ab} = Mutual inductance of the wiring loops terminating on Traces A and B

Note that the mutual capacitance between the loops that may have some effect on the potential difference between the traces is neglected. This assumption can be proved valid because of the long duration of the induced lightning pulses involved in this analysis. Also, a no-load termination between the adjacent traces has been assumed for further simplification in analysis and for further enhancement in the inter-trace potential difference.

In general, $e_a(t)$ and $e_b(t)$ may vary for wiring loops of different dimensions and for different categories of lightning environments. However, when the two cable interconnect wiring loops terminating on Traces A and B are in the same lightning environments and have equal loop dimensions, $e_a(t)$ and $e_b(t)$ can be considered equal ($e_a(t) = e_b(t)$).

As in the case of single-trace, common-mode induced voltages, for large values of the total loop terminating input and output impedances, both self- and mutual-inductance terms have an insignificant effect in limiting the induced lightning currents. The loops $I_a(t)$ and $I_b(t)$ are considered to depend primarily on the input and output trace impedances, yielding the following loop voltage equations:

$$e_a(t) = I_a(t)(R_{ia} + R_{oa}) \quad (8)$$

$$e_b(t) = I_b(t)(R_{ib} + R_{ob}) \quad (9)$$

For $R_{ia} << R_{oa}$, the sum

$R_{ia} + R_{oa} \cong R_{oa}$, and for $R_{ib} \rangle\rangle R_{ob}$, the ratio $\frac{R_{ib}}{R_{ib} + R_{ob}} \cong 1$

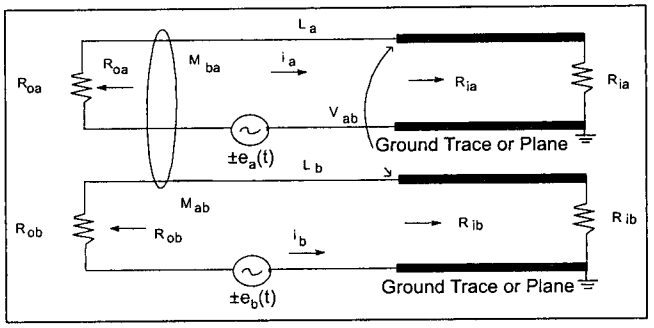

Figure 10. Two-trace induced lightning voltage theory.

Then the trace voltages become equal to

$$V_a(t) = I_a(t)\, R_{ia} = \frac{e_a(t)\, R_{ia}}{R_{ia} + R_{oa}} \cong e_a(t) \frac{R_{ia}}{R_{oa}} \quad (10)$$

$$V_b(t) = I_b(t)\, R_{ib} = \frac{e_b(t)\, R_{ib}}{R_{ib} + R_{ob}} \cong e_b(t) \quad (11)$$

The trace potential is then obtained as

$$V_{ba} = e_b(t) - e_a \frac{R_{ia}}{R_{oa}} \quad (12)$$

Assuming no common impedance within the loads at the end of the lines, both theoretical calculation and experimental results indicate that the inter-trace mutual capacitance has no effect on the R_{ia}/R_{oa} ratio.

In the case where $e_b(t) = e_a(t)$, the potential difference equation yields

$$V_{ba} = e_a(t)\left[1 - \frac{R_{ia}}{R_{oa}}\right] \quad (13)$$

Equation (13) indicates that when inequality relations $R_{ia} << R_{oa}$ and $R_{ib} >> R_{ob}$ hold, the potential difference between the neighboring traces may approach the wiring loop lightning-induced voltages.

EXPERIMENTAL VERIFICATION

In order to verify the potential differences which appear between circuit card traces, and to confirm the validity of Equations (4) and (13) derived in the theory, an experiment was performed using the wiring configuration and load termination found in a typical avionics cable. The 12-foot long avionics cable consisted of 13 wires terminated in typical circuit card input and output loads, such as protective diodes, 12-kohm resistors simulating ARINC 429 inputs, 10-kohm discrete inputs, small resistors and shorts simulating other input and output trace impedances (Figure 11).

The circuit card input and output impedances in each wiring loop were chosen so that at any typical trace, such as Trace A, the total loop impedance $R_{ia} + R_{oa}$ was larger than 12 kohm in order to simulate a typical avionics equipment. The large total impedance made the loop currents small, and therefore, the self- and mutual-inductance terms in Equations (9) and (10) are negligible as compared to the i_a $(R_{ia} + R_{oa})$ or i_b $(R_{ib} + R_{ob})$ terms. The list of input and output trace impedances is provided in Table 1.

The cable bundle was routed through a ferrite core coupling transformer with the cable wiring loops forming the inductively coupled turns of the transformer secondary. The wiring loop lightning-induced voltages were simulated by injecting pulses from a damped sinusoidal pulse generator connected to the single turn primary of a ferrite core transformer.

The pulse generator output was adjusted until an open-circuit peak voltage of 800 V at a secondary turn, small calibration loop terminal was recorded. In order to avoid the severe noise variations in the damped sinusoidal first peak, the 800-V peak voltage was referenced to the second peak. Nevertheless, a 2- to 5-percent variation in the peak voltage was noticed as the simulated lightning-induced voltages between the trace and ground, or between the traces, was measured.

With the trace input and output impedances acting as the transformer secondary loads, the damped sinusoidal pulses were injected into the cable wiring bundle. Trace potential to ground V_{ag}, V_{bg}, ... V_{mg} and the potential difference between traces V_{ab}, V_{ac}, ... V_{am}, V_{bc}, V_{bd}, ... V_{bm}, etc. was measured at the input wiring terminal using a storage oscilloscope with a differential input. The measured data for all the input traces (wire terminals) a, b, c, ... m, is provided in Table 2.

The effect of inter-trace potential differences causing arc and sparkover between traces was confirmed by connecting the traces on a circuit board to the cable bundle terminal pins, a, b, c, d, and f. The arcing and sparkover was initiated when the potential difference was increased and the electric field level for breaking down the inter-trace was reached. The effects of mutual induction between the cable bundle wiring was also investigated by increasing the current in one of the cable wires. The increased current in the wire, terminated on Trace *A*, was achieved by reducing the output impedance at Trace A to zero. The result of the experiment indicated that in a cable with 13 tightly bundled high-impedance wiring loops, the low impedance wire at Trace A reduced the trace voltage and inter-trace potential by approximately 4 dB. Further reductions of 6 dB and 12 dB in inter-trace potential differences were obtained by increasing the number of low impedance wires to 2 and 4 respectively. Based on these experimental results, no further significant reductions in potential difference could be reached, even when the number of low impedance wiring loops increased above 4.

Low-impedance wiring loops in the cable bundle are effective in inter-trace potential reduction only if they are in parallel with other cable loops in the same bundle. Any loop which terminates on circuit card traces through the same connector, but is not part of the main cable wiring bundle, may remain unaffected by the cable low impedance loops. This finding was supported by experiments and showed that the potential difference between Trace n and the main cable wiring traces will remain independent of the number of low impedance loops in the wiring (Figure 11).

SUMMARY

State-of-the-art circuit card operational function design has been concerned with common-mode voltages most often limited to 30 Vdc and differential voltages varying between -15 to +15 V. Lightning-induced voltages generated by the lightning environment result in common-mode

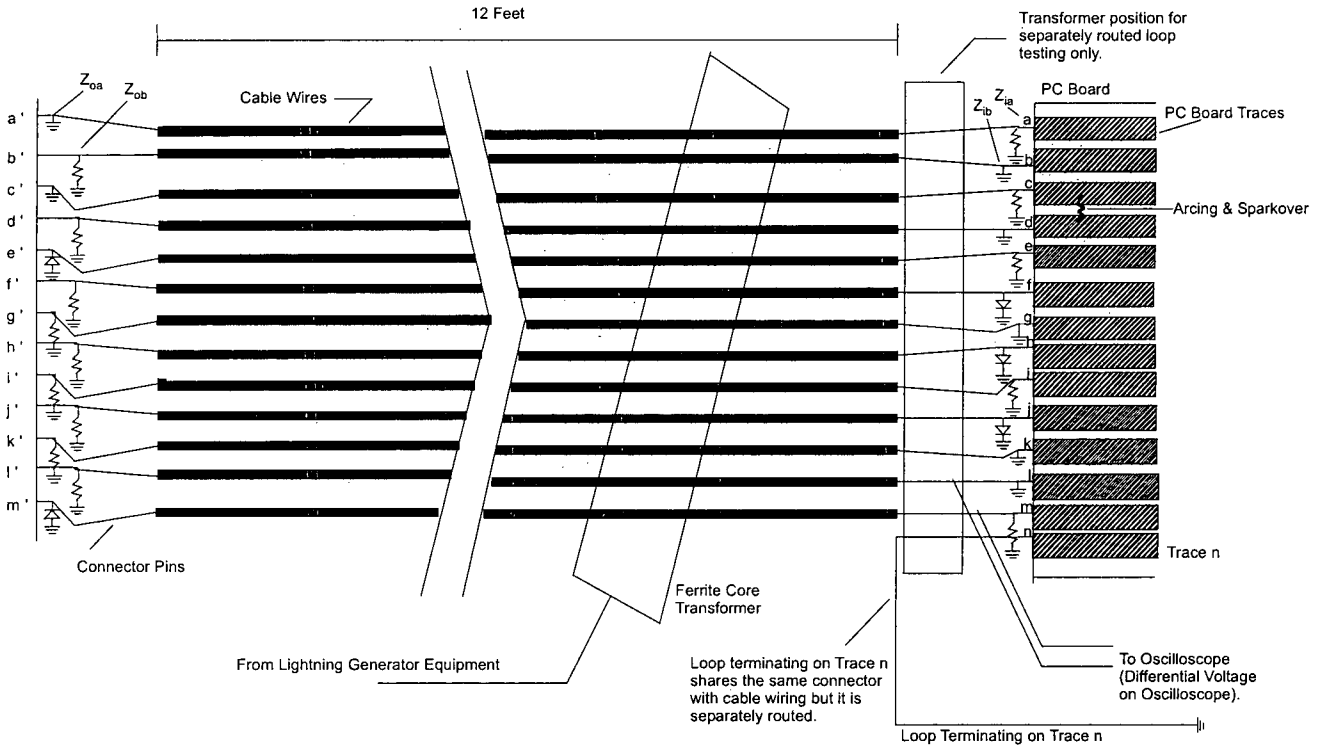

Figure 11. Twelve-foot cable bundle with 13 parallel cables and one cable not in parallel connected to terminating loads and PC board traces through wires simulating connector pins.

Trace Terminal	a	b	c	d	e	f	g
Input Impedance	12 kΩ	short	12 kΩ	short	12 kΩ	1N5646	short
Output Impedance	short	12 kΩ	short	12 kΩ	1N5646	12 kΩ	12 kΩ

Trace Terminal	h	i	j	k	l	m
Input Impedance	1N5646	10 kΩ	1N5646	short	short	12 kΩ
Output Impedance	10 kΩ	10 kΩ	12 kΩ + 1N5646	12 kΩ	12 kΩ	1N5646

Table 1. Input and output trace impedances.

Trace	a	b	c	d	e	f	g	h	i	j	k	l	m
P to Gnd V_{ag},... V_{mg}	800	0	800	0	800	44	0	46	<5	780	0	0	780
P to Trace V_{ab},... V_{am}		780	0	800	50	760	780	760	780	50	780	780	50
V_{bc},... V_{bm}			760	0	760	44	0	48	<5	780	0	0	760
V_{cd},... V_{cm}				800	46	780	800	760	800	45	800	800	45
V_{de},... V_{dm}					800	40	0	42	<5	780	0	0	780
V_{ef},... V_{em}						780	800	780	800	0	820	820	0
V_{fg},... V_{fm}							46	12	48	780	48	48	740
V_{gh},... V_{gm}								48	<5	760	0	0	780
V_{hi},... V_{hm}									42	780	40	760	760
V_{ij},... V_{im}										760	<5	0	780

Note: P = Potential

Table 2. Experimental data measurements.

voltages up to 1500 V peak which have often been suppressed to a maximum of 50 V peak using semiconductors, transistors, or varistors deployed as voltage clamping devices. Differential-mode voltages induced between the circuit card traces have been of little concern with respect to clamping, design safety, or component reliability evaluation.

This article proves, that as a result of new input and output impedances imposed on the circuit cards by the lightning protection devices and components in the lightning environment, the differential mode voltages which appear between the traces are significant and large enough that they should be clamped or their resulting electric field reduced. The results of the analysis indicate that inter-trace voltages can easily approach the magnitude of the loop voltages induced by the lightning. Since the wiring loop lightning-induced voltages in high lightning environments may reach 1500 V peak levels, carefully designed trace spacings and protective devices are required in order to prevent the adverse effects of sparkover between the circuit card traces as well as between the circuit card traces and the ground planes.

The accuracy of the theory has been proven by the experimental measurements provided herein. The evidence of the sparks appearing between the traces resulting from trace potential differences proves that protection of electronic components from lightning effects is important, as is protection of the circuit board itself.

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