CDM ESD Simulation in the Laboratory

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INTRODUCTION

Electrostatic discharge (ESD) is recognized as one of the major causes of failure of electronic devices. This article briefly explains the various ESD mechanisms — the human body model (HBM), machine model (MM) and charged device model (CDM) — and discusses how simulation of the CDM is accomplished in the laboratory.

WHAT IS CDM?

Integrated circuits (ICs) and similarly packaged devices can develop a self-charge. This usually occurs in today's automated factories when devices slide on conveyors or in shipping tubes during transportation.

Devices may also become charged by coming into contact with electrical ground while in an electrical field. Examples of commonly ocurring electrical fields in the real world are those brought about by cathode-ray tubes (computer monitors), charged insulators, humans and conductors. As soon as such a device makes contact with electrical ground, a charging pulse flows from the device to ground. This pulse charges the device and can damage it. If the device is electrically floating and removed from the electrical field, or the electrical field is collapsed, and the device is once again brought into contact with ground, a discharging pulse would flow from the device to ground, which can also result in damage to the device.[1]

HISTORICAL BACKGROUND

The CDM is not a newly discovered phenomenon. The earliest reference found on its occurrence dates to 1974,[2] but a final released industry standard does not yet exist for CDM. However, since the HBM standard[3] has been around for some time (Method 3015 .1 of MIL-STD-883 dates back to 1979), chip designers have been encouraged to build on-chip protection circuits to withstand HBM ESD only.

The charged device model has emerged as the dominant ESD cause of IC failures.

Figure 1 shows the schematic diagram for the HBM. Basically, the human body is modeled to have a capacitance of 100 pF in series with a resistance of 1500 ohms. This capacitor is first fully charged to a specified voltage and then discharged through a 1500-ohm resistor into the device under test (DUT).

The MM is believed to have been first created in Japan in 1976 and is incorporated in a standard published by the Electronic Industries Association of Japan. This standard uses 200 pF, 0 ohms as the human body model. The industry at large began to refer to this as the machine model to distinguish it from the human body model, and the name has stuck. Figure 2 shows the schematic diagram for the MM.

DISTINCTION BETWEEN CDM AND HBM/MM

The main distinction between the CDM, HBM, and MM is that in the CDM, energy flows from the device to ground, whereas in the HBM and MM, energy flows from a human being or machine to the DUT. The energy in the CDM flows from the capacitance created between the device and its surroundings, whereas in the HBM and MM, an external capacitor is made to discharge into the device. The CDM can be regarded as reverse ESD, or more specifically, reverse MM.

IMPORTANCE OF CDM SIMULATION

In his 1982 paper, Unger[1] argued that "although the industry appears to be concentrating on the evaluation of ESDs from the human body model ... ESDs described by the charged device model are at least as likely and possibly more likely than the HBM discharge." Due to rapid introduction of automated device handling machines, CDM damage has become the major ESD-related failure of integrated circuits since 1985 or 1986.[4,5]

CDM SIMULATOR TECHNOLOGIES

Three distinct types of simulators, each with specific advantages and disadvantages, have emerged for CDM testing. These are: chip-in-socket, dead-bug direct charging and dead-bug field induced charging. The features of these simulators are discussed below.

CHIP-IN-SOCKET

This method uses a typical tester DUT interface board. The chip is plugged into the socket as it

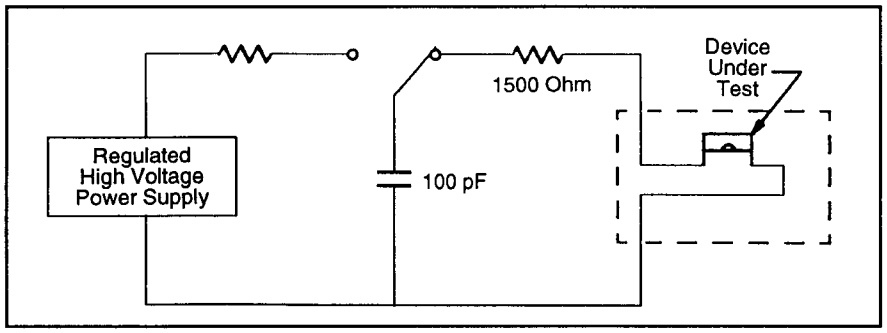

Figure 1. *Circuit Schematic of Human Body Model Testing of Devices for ESD Susceptibility.*

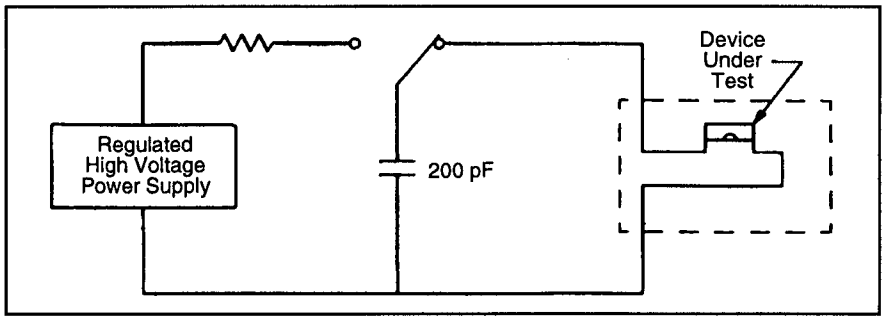

Figure 2. *Circuit Schematic of Machine Model Testing of Devices for ESD Susceptibility.*

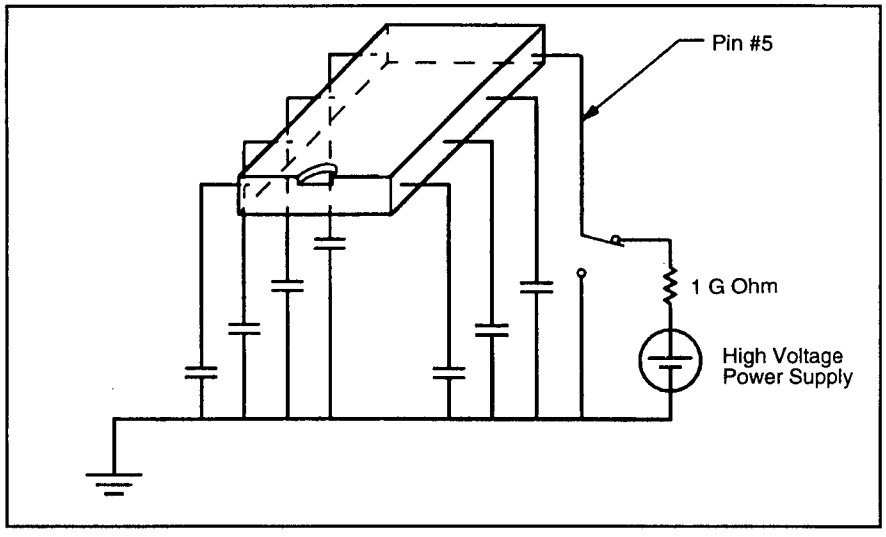

Figure 3. *Chip-in-socket Type Relay-based CDM Simulator. The relays are depicted by their equivalent capacitances.*

normally would be. One of the pins is connected to a high-voltage power supply while charging. All the other pins are floating. The charging process usually takes a few milliseconds due to the series resistance of the high-voltage supply and the chip, and the capacitance of the chip. Once the chip is fully charged, one of the pins is connected to ground as the high-voltage supply is removed from the charging pin.

To be able to test each pin of the device for charging and discharging, the tester uses a relay matrix type. Each of the relays which is open will have an equivalent capacitance. Figure 3 illustrates a circuit schematic for testing of an 8-pin device, with the relays depicted by their equivalent capacitances. To simplify this example, the relay for pin # 5 is depicted as a two-way switch. Each time the device is charged, it is not only the capacitance of the device, but also the relay capacitances which get charged. The capacitance of the device is small, usually on the order of 1 to 40 pF. The capacitance depends on the size of the chip, and is low for smaller chips. With low chip capacitances, the combined capacitances of the relays become significant. Typical capacitance of each relay is about 1 to 3 pF. Also, for the larger chip with more pins, since there is at least one tester relay per pin, the combined tester relay capacitances increase with the increase in the number of pins.

Relay capacitances are a serious disadvantage for this type of simulator. The average number of pins per integrated circuit increases every year, and this trend is expected to continue as higher levels of integration are achieved within the IC, and the semiconductor industry moves from VLSI to ULSI. Relay capacitances, introduced by the tester, are considerable for ICs with more pins. Even for lower pin count ICs, relay capacitances are a significant fraction of chip capacitance.

DIRECT CHARGE, RELAY DISCHARGE SIMULATOR

To circumvent the parasitic tester relay capacitances associated with chip-in-socket, this method places the chip on a test table with pins facing up in the dead-bug position. The chip is charged by a mechanical probe coming in contact with one of its pins. It is discharged through a relay which connects with one of the pins on the chip. Major disadvantages of this setup, depicted in Figure 4, are the discharge relay capacitance and discharge path inductance. Although inductance outside of the relay has been highlighted in Figure 4, it is the length and geometry of the moving contact of

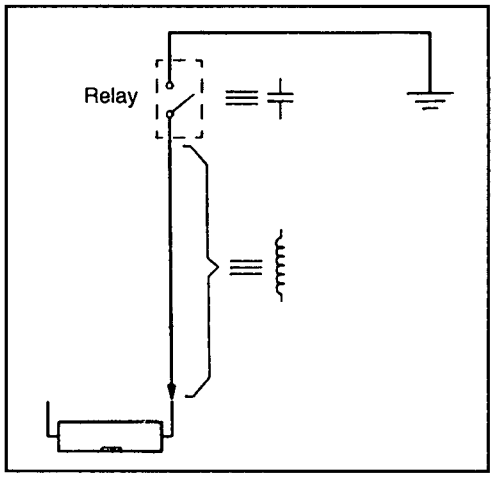

Figure 4. *Discharge Path in a Direct-charge, Relay Discharge Simulator. The equivalent capacitance of the relay and inductance of the long discharge path is highlighted.*

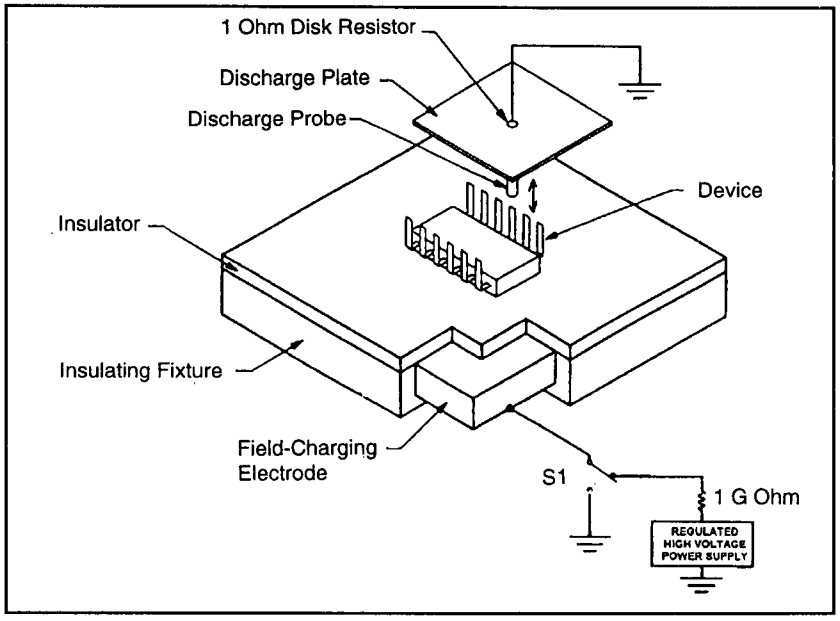

Figure 5. *Schematic of FCDM (Field-induced CDM) type of Simulator.*

any relay which is the main contributor to inductance. The charging probe circuitry has been omitted from this figure for simplicity. Note that capacitance of the charging probe would also be an additional tester-induced parasitic.

FIELD-INDUCED CHARGED, DIRECT DISCHARGE SIMULATOR

The schematic for a field-induced charged, direct discharge simulator is shown in Figure 5.[6] The device is charged by being in the presence of an electric field created by the charging electrode. After a few milliseconds, the discharge probe is brought down to make contact momentarily with one of the pins, resulting in the charging pulse. The DUT is now charged and can sustain CDM damage due to this charging pulse.

Next, the field is collapsed by connecting relay S1 to ground. The device still remains charged and a second CDM pulse occurs when the probe is brought down once again to make contact with one of the pins. This is the discharging pulse which can cause damage to the device.

A large ground plate (discharge plate), about 3 x 3 inches square, is placed very close to the tip of the discharge probe. This significantly reduces discharge path parasitic inductance and capacitance associated with the relay discharge type of simulator discussed in the previous section. From the physics point of view, the large ground plate acts as a charge sink.

Many believe that the field induced charged device model more accurately reflects "actual" ESD events in the factory: "The FCDM (Field-Induced CDM) simulator is more like the major factory processes that cause ESD failure than simulators that use direct charging, because few such processes directly charge a device's pins."[7]

A draft standard for CDM testing, developed by The ESD Association, is being used and evaluated at the present time.

SUMMARY

Various failure mechanisms due to ESD, including HBM, MM and CDM, were explored. Simulator technologies for CDM, the newest test model for ESD, were discussed. It is believed that with the automation of manufacturing and testing processes, CDM emerged as the dominant ESD cause of failure for integrated circuits. A draft standard for CDM testing has been developed.

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