A SYSTEMS APPROACH TO ESD TESTING

Instrumentation

A systems approach to ESD simulation requires an overview of six major areas:

- test philosophy,
- test parameters,
- single-shot vs. repetitive testing,
- monitoring,
- calibration,
- safety.

Test Philosophy

No precise model exists for replicating the ESD effects of human anatomy on an intended environment; the variability factor is too great for replication. There are, however, five major disruptive effects of body-generated discharge: pre-discharge, corona-generated RFI; pre-discharge electric field; discharge electric field collapse; the discharge magnetic field, and current-injected standard waves. It is possible to simulate conditions to produce these effects, and measure the results.

Separate, standardized simulation of all five effects offers an eventual path to repeatable ESD test instrumentation. No such standards are now available. Although standardized, directly-injected waveforms are appealing for their uniform, shot-to-shot characteristics, a simple air discharge is closer to reality.

A recommended testing approach is to compromise — using air discharge tests in engineering, standardized waveform injection for production and quality control work, and corona and field generators in investigative, diagnostic, and R&D activities.

Test Parameters

Human-Body Models. The simplest and presently the only generally-accepted human-body model is a single capacitor, discharging via a single resistor. Figure 1 shows a sample network model for the human body, with the range of values suggested in the literature. Figure 2 shows the IEC-recommended values.* More complex models have been proposed to simulate multiple discharge effects, as well as more complex body models that may result in much faster wavefronts and narrow overshoot phenomena.[6-9] Figures 3 and 4 show examples of more complex models.

In view of the higher-density device technologies rapidly coming on stream—GaAs, SOS, lithography, and so on, it's likely that more complex body models will be needed to insure adequate testing of their increased sensitivity to the ESD event.

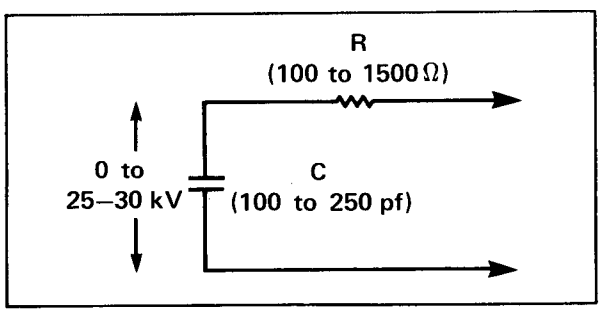

Figure 1. Basic, Single-RC ESD Model for the Human Body.

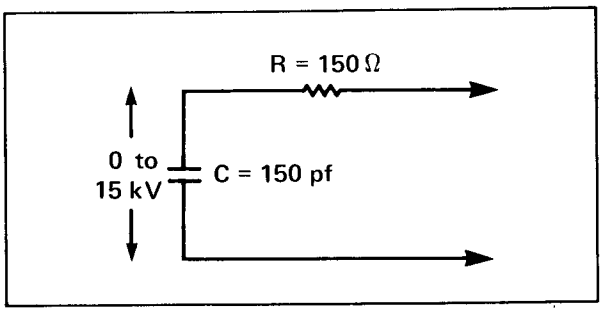

Figure 2. IEC Values for the Single-RC ESD Model.

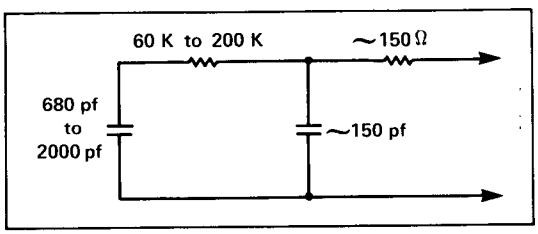

Figure 3. Multiple-Pulse Model For an Upper/Lower Body Configuration.

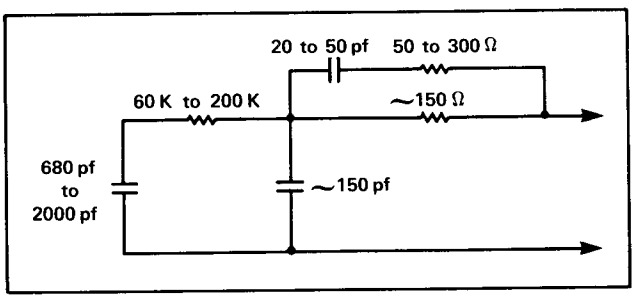

Figure 4. Extended Multiple-Pulse Model Including Initial-Edge Sharpening and Overshoot Production.

*The IEC is the International Electrotechnical Commission, an international standardizing organization. Working Group 4 of IEC Technical Committee 65 has pioneered a draft Standard ESD (see Ref. 10).

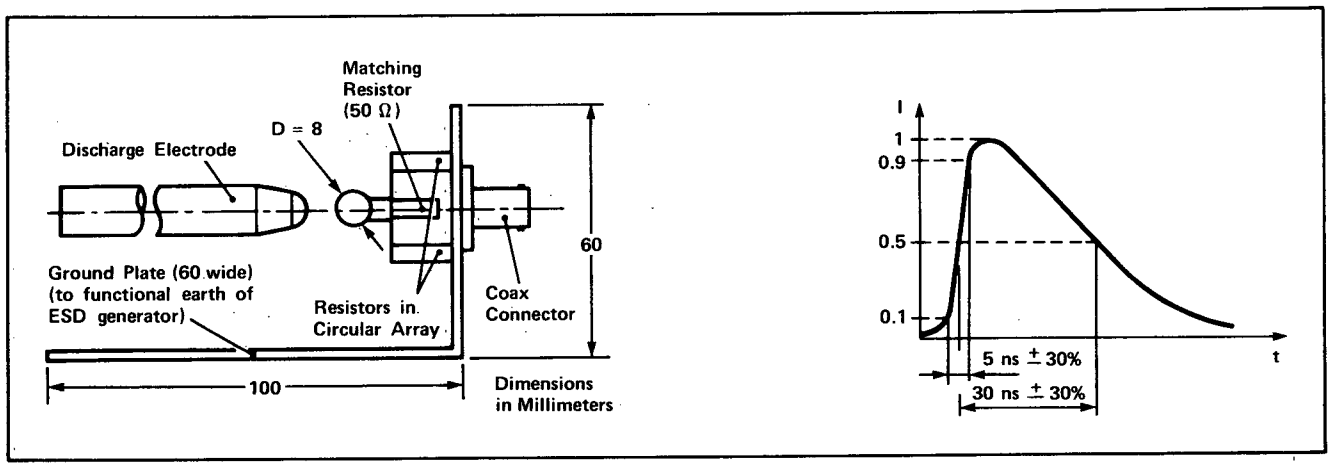

Figure 5a. IEC Coaxial "Target" Current Calibrator.

Figure 5b. IEC-Specified ESD Waveform.

Maximum Test Voltage. Suggested maximum test voltages range from 15 to 30 kV. IEC TC65/WG4 [10] has opted for the 15 kV low end. It would seem clear from the literature that a figure between 20 and 30 kV is a more realistic test limit, with 25 kV perhaps a likely candidate.[11-15]

Test Voltage Polarity. Both polarities of ESD occur in practice,[9, 15, 16] and bipolar semiconductor devices like op amps are more than an order of magnitude more sensitive in one direction (reverse bias) than in the other.[17-22] The IEC draft specification calls for a unipolar, positive output. An eventual change to a bipolar ESD test requirement would seem inevitable.

Single-shot vs. Repetitive Testing

Repetitive testing is necessary to insure a statistically valid check on ESD sensitivity vs. internal timing cycles in the EUT (equipment under test). Hundreds of tests must routinely be run to achieve this. Thousands, or in extreme cases, even tens of thousands may be required, depending on the EUT and the economic and product marketing stakes involved. There are limitations however. Too high a test rate can damage devices due to excessive average power. The fact that a tester can be designed to run at 1 kHz isn't a reason to do so; in fact, the IEC "exploratory" rep rate of 20/second can be too high in many circumstances. Table 1 shows the average power in multiple discharges.

Average Power for Repetitive ESD Testing

CAPACITANCE and VOLTAGE CATEGORY	C (pf)	kV	ENERGY/ SHOT (milli-joules)	POWER at 1 SHOT per 3 SECONDS (mw)	POWER at 20 SHOTS per SECOND (mw)
DISTRIBUTION EXTREME	500	40	400	133	8000 ! ! !
REASONABLE WORST CASE	250	25	78	26	1563 ! !
TYPICAL (IEC MAXIMUM)	150	15	17	6	338 !
MINIMUM PROTECTION	100	6	2	1	36

Table 1. Average Power for Repetitive ESD Testing.

Monitoring

As in all surge testing, instrumentation used to monitor delivered wave parameters is critical to a successful test program. Monitoring should include:

a) display of the high voltage to which the high-voltage capacitor will be charged when the high voltage switch is depressed. This guarantees there'll be no surprises, a desirable assurance in high-voltage work.
b) measurement and display of the actual high voltage standing on the high-voltage capacitor after the high-voltage switch has been depressed, as actually measured across the capacitor.
c) measurement and display of the voltage on the high-voltage capacitor after discharge, so the operator knows the discharge has occurred.
d) measurement and display, or availability for display, of the current delivered during the discharge. While the data is probably not necessary during routine ESD testing, discharge current is a crucial indicator of circuit inductance, protector operation and circuit degeneration as a result of repeated ESD's. Since these are waveform phenomena, a precision current output for scope monitoring is the indicated mechanism.

Calibration

All instrumentation requires periodic checks and calibration. This is critical for high-voltage test equipment, which applies extra high stress to internal components, having a higher probability of internal drifts and failures.

An ESD tester should have auxiliary, independent calibrators for all the simulated ESD effects. If the tester is limited to air discharge, it should have a coaxial "target" load for scope calibration of rise time, decay time and peak amplitude. IEC TC65/WG4 defines such a calibrator, for example, with construction details. Figures 5a and 5b give an idea of what the calibrator and a typical wave form look like.

ESD testers that have capability for independent simulation of one or more of the five major components of the air discharge should be equipped with capability for calibrating them. The coaxial target load used for air discharge wave calibration is sufficient for directly-injected current. Additional sensors for the other four phenomena are also preferred.

Safety

Pacemakers, electronically-controlled machinery, and similar medical and/or production equipment may malfunction during an ESD test, even though located some distance from it. Suitable precautions should be taken. ESD test equipment should meet certain basic requirements that are related to both safety and good practice.

1. An ESD simulator in single-shot mode should discharge rapidly and automatically when the high-voltage switch is released and/or the unit is put down.
2. When high voltage is required, it should be continuously measured and displayed.
3. If the operator decides to reduce the high voltage to a lower level after charging up the output capacitor, the high voltage should "track" the high-voltage control downward as its setting is reduced; otherwise, discharge will be required to bring the voltage down. A corollary is that all internal high-voltage capacitors should have built-in shunt resistors, to assure discharge in just a few seconds when power is turned off.

The test equipment user also has certain obligations related to safety and good practice. They include:

1. Connecting the ground strap. Ungrounded testing shouldn't be necessary.
2. Calibrating the ESD tester on a reasonable, routine basis. The high voltage that appears should be the high voltage dialed up. The output pulses, fields and corona should also be checked. Calibration equipment for all key parameters should be acquired either from the ESD simulator's manufacturer, or independently.

The ESD Test Program

Purpose of the Tests. There is a vast difference between the exhaustive ESD testing of a prototype computer destined for sales in the tens of thousands of units, and the routine, AQL verification of a process controller shipped at the rate of five or six a month. With the high-volume computer, repetitive ESD testing may have to be carried out while the machine runs in check-sum, parity and/or computational modes and prints out its own resulting errors. With the AQL test on an already designed, lower-volume machine that's giving no known ESD trouble in the field, it may be sufficient to re-check previously-identified weak spots and then merely spot-check for a few others.

Technologies Used in the Equipment Being Tested. If the system under test involves only standard power TTL, serious ESD problems are unlikely. Low power Schottky, CMOS and the newer technologies are another matter. Table 2 shows the ESD sensitivity hierarchy.[23]

ESD Sensitivities for Various Technologies

DEVICE TYPE	RANGE of ESD SUSCEPTIBILITY (Volts)
VMOS	30–1800
MOSFET	100– 200
GaAsFET	100– 300
EPROM	100
JFET	140–7000
SAW	150– 500
OP–AMP	190–2500
CMOS	250–3000
SCHOTTKY DIODES	300–2500
FILM RESISTORS (THICK, THIN)	300–3000
BIPOLAR TRANSISTORS	380–7000
ECL	500–1500
SCR	680–1000
SCHOTTKY TTL	1000–2500

Table 2. *ESD Sensitivities for Various Technologies.*

Tests should be performed with the equipment both mounted on and then isolated from a ground plane; in all operating modes; in all equipment configurations. Testing should be started at low voltages, increasing the voltage in steps after each group of shots. Finally, if the EUT can self-monitor, repetitive testing at a slow rep rate should be set up, including a pass/fail limit. Testing for a period of time that will give meaningful statistical results in terms of machine-timing sensitivity to ESD coincidences is important.

Testing should be performed at points carefully selected as part of the test plan. Specific discharges should include the following:

a) the ground plane when it is used;
b) the sides, front and rear of the equipment enclosure;
c) all crucial keys—reset, run, etc.,—and at least some of the alphas and numerics;
d) all controls;
e) all displays;
f) all cables, both data and power.

Indirect, field-induced effects can then be checked by discharging the tester into its own return line, with the discharge in close proximity to the EUT. This kind of testing should be done for different arc discharge orientations versus the EUT, and can be carried out at high rep rates.

If corona and field generators, plus current injection are available, then failure diagnostics will be substantially improved. In particular, re-checking on an AQL basis can become a highly precise affair. For example, if a printer head resets to zero or a memory is erased with a 10 kV air discharge to the side of the cabinet, it is possible the same effect may occasionally occur at 5 kV, and may not always happen at 15 kV. However, if the effect results from a direct current injection, or from E-field collapse or H-field generation on discharge, it should be reproducible within a kV or so, given the right equipment to individually simulate the various air-discharge effects.

ESD Threats the Equipment Must Survive in Use. Electronics intended for an air-conditioned, humidified environment may require testing at lower levels than systems to be used in uncontrolled conditions. The IEC draft Standard[10] defines various application levels, or classes, in an attempt to make this kind of distinction. Table 3 gives the four classes the IEC defines.

ESD Test Voltages versus Equipment Application Classes in Draft Standard IEC TC65/WG4 Part 5

CLASS	RH CONTROL	RH%	ANTISTATIC CARPET	ESD TEST kV
1	YES	>50	YES	2
2	NO	<50	YES	4
	YES	>50	NO	4
3	NO	30 To 50	NO	8
4	NO	<30	NO	15

Table 3. EST Test Voltages vs. Equipment Application Classes in Draft

Implications of the Latent Failure Problem. ESD has the potential for delayed reactions within sensitive microcircuits that won't become evident for months or even years.[24-29] These delayed-reaction failure mechanisms show up as ghost bits, check-sum failures, bit dropouts and the like; and severely plague those designs that push their internal semiconductors to the limits of their speed and other performance capabilities. At the engineering and prototype level, it is necessary to learn the amount of voltage (or energy) above the limit the equipment is supposed to meet, that will actually cause failures. Knowing design margin, and even tracking it on an AQL basis over time after the product is in production, can prevent surprises. The result can be knowledgeable control—from an ESD standpoint—of the production process.

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