


emc13bga CCC

Suppressing ICs with BGA packages and multiple DC rails



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interference
technology

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Some Intel Core™ i5 BGA packages



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A Xilinx FPGA in BGA packaging



XILINX
VIRTEX-7
XC7V2000T
FLG1925ACX1133
AA20845A

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High-Performance High-Density Silicon-proven IP

ON Semiconductor's internal 110nm process technology, using BGA packaging, that they use for ASICs

1.2V
110nm

ON
SP110

Cell based ASIC

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Creating good planes under BGAs

- For cost-effective SI, PI and EMC, it is important to have solid PCB planes *underneath the ICs...*
 - unfortunately, through-hole-plate (THP) PCB technology means an array of via holes under all BGAs...
 - which dramatically perforate the planes and significantly reduce their effectiveness for EMC...
 - and also harm signal integrity (SI) and power integrity (PI)
- Two solutions:
 - High Density Interconnect technology (HDI, = microvia)...
 - fine-line THP techniques, to create proper meshes

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High Density Interconnect (HDI) PCB manufacturing technology

- Also known as microvia technology, or Sequential Build-Up technology (or simply 'Build-Up')
- Based on 'microvias' of 0.15mm (6 thou) diameter or less, which are only as long as needed...
 - and don't steal solder during reflow, so allow *via-in-pad* layouts, very good for RF and EMC...
 - can achieve twice the number of pins/area than THP...
 - can significantly reduce the number of PCB layers *especially* where THP would require 10 or more layers

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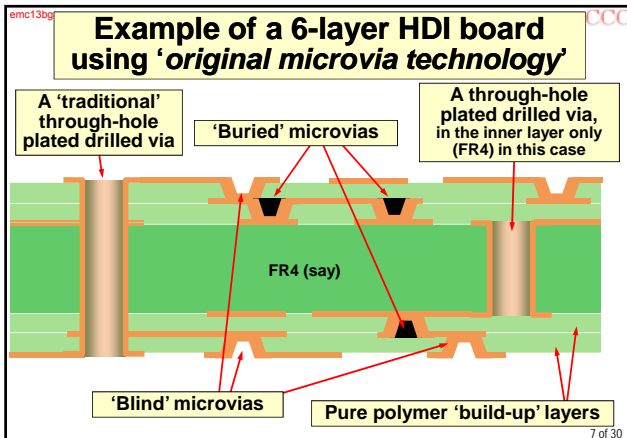


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- HDI benefits**
- HDI techniques help to make the smallest, lightest, and least power-hungry products...
 - and can be found in a wide variety of common products (including some toys)
 - HDI makes it possible to use the smallest IC package styles, e.g...
 - Miniature or Micro BGA (especially with ball pitch <1mm)
 - DCA (direct chip attach)
 - Flip-chip
 - CSP (chip scale packaging)
 - TAB (tape automated bonding)

- HDI benefits continued...**
- These small ICs, and the smaller PCBs they allow, are generally excellent for SI and EMC...
 - via-in-pad reduces decoupling inductance and pushes resonant frequencies higher...
 - shorter traces make less efficient 'accidental antennas'...
 - smaller PCBs resonate at higher frequencies...
 - the much smaller sizes of the ICs and their close proximity to a solid 0V plane means they emit less...
 - shorter traces may not need to be transmission lines

- HDI's planes aren't perforated**
- So they have lower impedances...
 - hence lower emissions and better immunity...
 - and they have constant return path inductance...
 - for improved Z_0 control of transmission-lines...
 - and they achieve better shielding between the circuits on the top and bottom sides...
 - e.g. digital on top, analogue/RF on the bottom...
 - and they create solid, continuous planes under BGAs...
 - so help reduce the specs of filtering and shielding

- HDI suppliers and technologies**
- In May 2000 there were 62 manufacturers of HDI boards worldwide, and in May 2008 there were 32 manufacturers just in the UK...
 - their manufacturing techniques can vary, and may need different layout techniques, so always check with chosen manufacturer *before* starting board layout
 - Basic standard: IPC-2315 (from www.ipc.org) ...
 - but HDI requires a different approach to PCB layout...
 - and – depending on the supplier – some PCB EMC techniques might not be able to be used

- People seem to think that HDI is costly, but it should cost less than THP!**
- An IPC survey in 2000 found HDI boards could be purchased for the same cost as THP...
 - and not using buried vias helps reduce costs further
 - Latest advice (Mentor Graphics) is that boards needing > 8-10 layers should cost less if made in HDI...
 - e.g. a high-density 18 layer THP would only need 10 layers if made using HDI...
 - but even lower densities and with fewer layers, the EMC (and SI) advantages of HDI make it more cost-effective than THP



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Modern HDI PCB technology

- has many advantages over 'original' HDI...
- and is the topic of my next webinar, on September 17

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Fine-line THP techniques

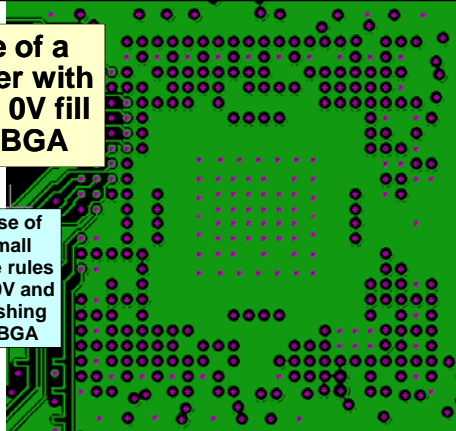
- We must *at least* achieve a continuous mesh (grid) of 0V and power traces under every BGA...
 - to connect all their 0V and PWR power pins to their respective decaps...
 - and to the 0V and PWR planes on the rest of the board...
 - and to help control emissions
- It won't be half as good for EMC as a solid plane (e.g. using HDI)...
 - but it will be the best we can do in THP

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Example of a signal layer with a meshed 0V fill under a BGA

Showing the use of adequately small track-and-space rules to create good 0V and PWR plane meshing underneath a BGA



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Planes under BGA devices continued...

- BGAs with ball pitch ≥ 1 mm can create continuous meshes underneath...
 - using 175 μ m (7 thou) track-and-space (track-and-gap)
- BGAs with pitches 0.8 - 1.0 mm need 100 μ m (4 thou) track-and-space to create a mesh...
 - NOTE: for several years now, 100 μ m offshore volume-manufacture now costs no more than 175 μ m
- And BGA pitches 0.5 - 0.8 mm need 50 μ m (2 thou)...
 - some UK PCB manufacturers can do this (e.g. Merlin Circuit Technology)

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Poll Questions

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Where an IC has multiple DC rails

try to get all of its power planes on one board layer

Segregate each circuit area that is powered from a different voltage (i.e. locate all components and route their traces within that plane's area)

Solid 0V plane under all power planes, and extending beyond them

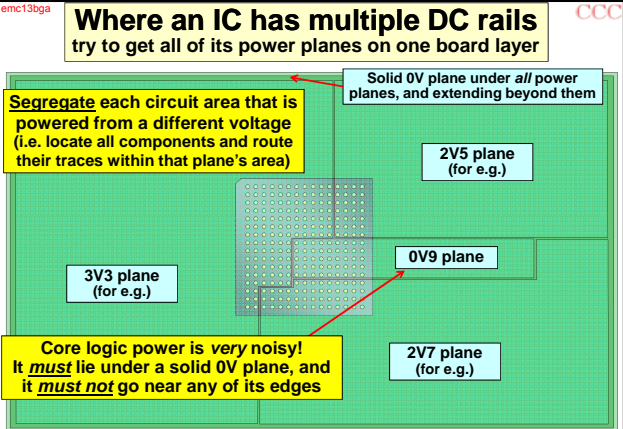
3V3 plane (for e.g.)

2V5 plane (for e.g.)

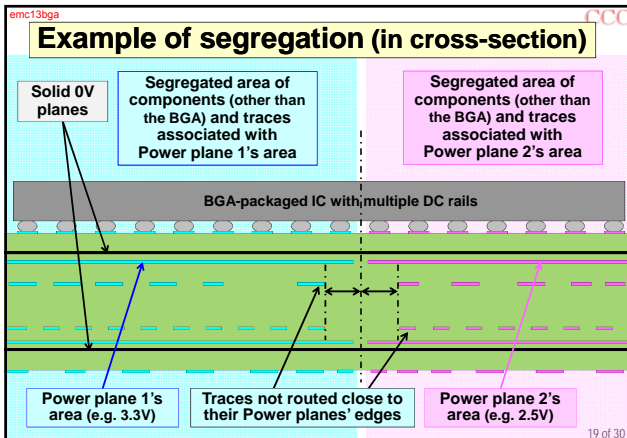
0V9 plane

2V7 plane (for e.g.)

Core logic power is very noisy! It *must* lie under a solid 0V plane, and it *must not* go near any of its edges



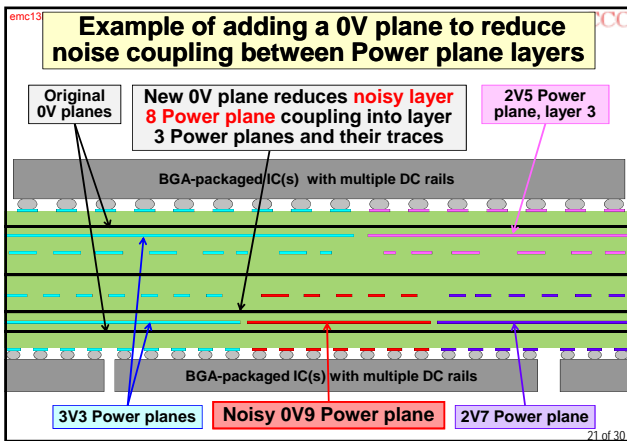
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Reducing the crosstalk between PWR planes on parallel layers

- To help prevent RF noise in a 'noisy' plane...
 - e.g. processor core logic supply, typically 0.9 – 1.2V
- from coupling its noise into parallel power planes and spreading more widely around a board...
 - increasing emissions...
- place a new 0V plane between them in the stack-up

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Reducing crosstalk between PWR planes on parallel layers continued...

- 'Sandwiching' a power plane layer between two solid 0V planes as in the previous graphic...
 - also means no trace routing has to worry about crossing any splits between different power plane areas...
 - and can double the power planes' buried decoupling capacitance...
 - which helps suppress emissions at >300MHz

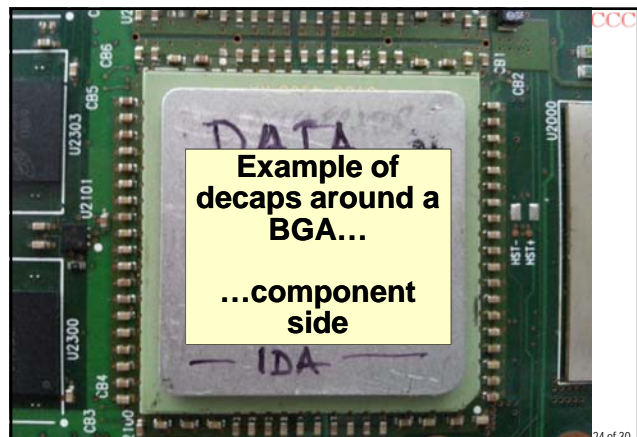
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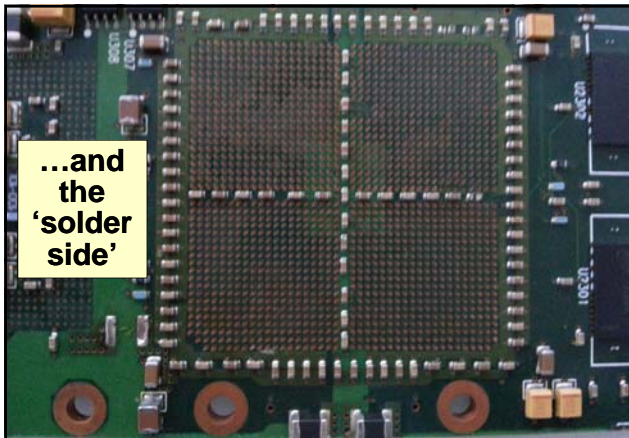
Copper-filled/capped vias can ease routing under BGAs...

- by replacing 'dog bones' with via-in-pad...
- bare board cost increases by about +10% (in volume)...
- prototypes can use high-temperature solder to save cost

No pin-escapes or 'dog bones' !!

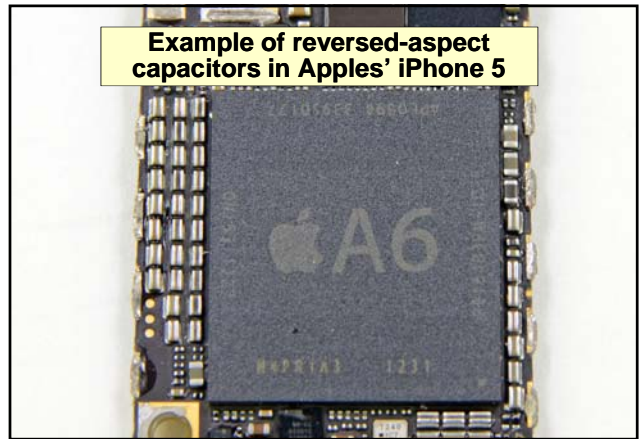
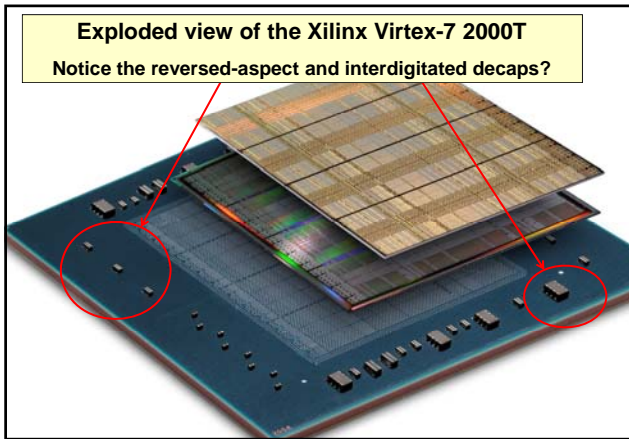
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Special capacitors with reduced ESL can improve Power Integrity, e.g...


- 'reversed-aspect', e.g. 0204, 0508, Murata LLL, etc...
- 'interdigitated', e.g. AVX IDC, LICA; Murata LLA, LLM...
- balanced X2Y® capacitors used as decouplers...
- lossy capacitors dampen resonances, e.g. Murata LLR
- buried capacitors, e.g. Murata GRU...
- distributed 'embedded' capacitance using proprietary board laminates for one or more pairs of PWR/GND planes, e.g...
 - Faradflex (Oak Mitsui); ECM (3M); Interra™ HK 04J (Dupont); EmCap® (Sanmina), and others



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the end

interferenceTM
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