Digital Circuit Radiated Emission Suppression With Spread Spectrum Techniques

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INTRODUCTION

Meeting the regulatory requirements is becoming increasingly difficult for many electronic products. Microprocessors are becoming faster, and with this increased performance comes increased radiated emissions due to the higher frequencies present in the system. Often, the primary sources of radiated emissions which exceed the regulatory limits include the microprocessor, the oscillator circuits, and derived signals such as address or data buses. Filter components could be added to signals to increase their rise or fall times and thus reduce the high frequency content. However, with microprocessors having 32-bit wide data and address buses, filtering more than a few of these lines is often physically impossible due to space constraints. Any method which would *simultaneously* reduce the emissions from *all signals* associated with a microprocessor or microcontroller could significantly reduce the cost of complying with the regulatory requirements. A technique to accomplish this goal has recently been developed.[1,2]

A method which simultaneously reduces the emissions from all microprocessor signals would reduce the cost of compliance.

In the late 1940s, development began on a communication technique to intentionally broadband a radio signal without increasing the modulation. This technique has come to be known as *spread spectrum* transmission.[3] The initial design objective of this technique was secure, jamproof military communications. It is still used extensively for this purpose although commercial communication applications have also been developed. The technique described here is analogous to these communication spread spectrum techniques by the spreading of the energy in the intended signal. The primary clock used to provide timing signals to a microprocessor or other digital circuit is intentionally broadbanded to reduce the amplitudes of radiated emissions that are the result of this clock signal or any signal synchronized to it. This technique is hereinafter referred to as *Spread Spectrum Clock Generation*, or SSCG.

In a typical microprocessor-based system, an external oscillator or clock generator is used to provide the fundamental timing signals. Since the signal is approximately a trapezoidal pulse train, harmonics are present at each integer multiple of the fundamental frequency. For example, consider a trapezoidal clock signal with a fundamental frequency of 15 MHz. Harmonics of this clock signal are found at integer multiples of 15 MHz with the amplitude of the harmonics dependent upon the pulse rise and fall times and the pulse width. For a pulse train with a 50% duty cycle, only the odd harmonics are non-zero. However, it can be shown that even slight deviations from a duty cycle of 50% result in significant even harmonics. Deviations in the duty cycle can be caused by temperature or load variations, and can vary significantly over brief periods of time.

In the frequency domain, harmonics of the trapezoidal clock signal are represented as delta functions at each harmonic frequency (Figure 1). The data presented in Figure 1 are actual spectral data measured with a spectrum analyzer. The center frequency of the spectrum analyzer is set to 315 MHz, which corresponds to the 21*st* harmonic of the fundamental frequency. The SSCG modifies the spectrum of the clock signal by *frequency modulating* (FM) the clock signal. With SSCG, the spectrum of the clock signal is changed from a delta function concentrated at the frequency of the *nth* harmonic to a series of sideband harmonics, centered over the frequency of the *nth* harmonic, but spread over a much wider frequency span, thereby reducing the amplitude of the harmonic. The separation of the sideband harmonics is given by the frequency of the modulating signal.[4] As shown in Figure 1, by applying the SSCG technique to the 15 MHz clock signal, the peak signal of the 21*st* harmonic is reduced by approximately 10 dB when compared to the standard non-modulated signal.

The degree of attenuation provided by SSCG is dependent

upon the maximum frequency deviation and the shape of the waveform used to frequency modulate the clock signal. The 15 MHz clock of Figure 1 is modulated with a 30-kHz signal and the peak deviation is ±100 kHz. At the 21*st* harmonic, the spread of the resulting harmonic will be given as

$$2 \times 100 \text{ kHz} \times 21 = 4.2 \text{ MHz}$$

Since the spread increases with each harmonic, the attenuation provided by SSCG increases with frequency.

It is important to note that although the SSCG technique consists of frequency modulation of the clock signal, the waveform used is not typical. Standard waveforms such as a sine wave provide little if any attenuation. However, the modulating signal was empirically derived and provides optimum attenuation.[1,2] The amplitude of the modulated harmonic is nearly uniform across the span of the harmonic (Figure 1). This is critical to optimizing the attenuation provided by SSCG.

MEASURED RESULTS

In order to verify the attenuation provided by SSCG, the experimental implementation shown in Figure 2 is used. The synthesizer generates the frequency modulated SSCG signal with a unique modulating waveform generated by an arbitrary waveform generator. The output of the synthesizer is amplified and converted to a 5-volt square wave by a zero-crossing detection circuit. The attenuation can be measured with a spectrum analyzer or quasi-peak receiver directly, or the signal can be transmitted via a fiber optic link to the printed circuit board of an actual electronic product. By setting the peak deviation to zero, a standard clock signal is provided by the synthesizer.

The attenuation provided by SSCG is found by measuring the peak amplitude of each clock harmonic with and without modulation. The attenuation at the *nth* harmonic is defined as the ratio of the peak amplitude of the *nth* harmonic without modulation to the peak amplitude of the harmonic with modulation. This attenuation will be the same regardless of the detector used; that is, whether a quasi-peak detector or the peak detector of a spectrum analyzer is used. The attenuation in dB measured using the configuration of Figure 2 for fundamental clock frequencies of 20 MHz, 32 MHz, and 40 MHz is found in Figures 3 through 5, respectively. Data for two deviations, ±100 kHz and ±250 kHz, are given.

The attenuation values found in Figures 3 through 5 have an initial value of approximately 0 to 1 dB and increase with frequency at a slope of 10 dB/decade. The attenuation obtained with a peak deviation of 250 kHz is approximately 3 to 4 dB greater than the attenuation obtained with a peak deviation of ±100 kHz.

At the higher frequencies in Figures 3 through 5, a wide variation in the attenuation is observed, with the greatest variation at a peak deviation of ±250 kHz. The lower attenuation values occur at those frequencies which, in the case of the nonmodulated clock signal, correspond to nulls in the Fourier series expansion of the trapezoidal pulse train. This variation in the attenuation is the result of the frequency modulation of the clock signal shifting the frequency of

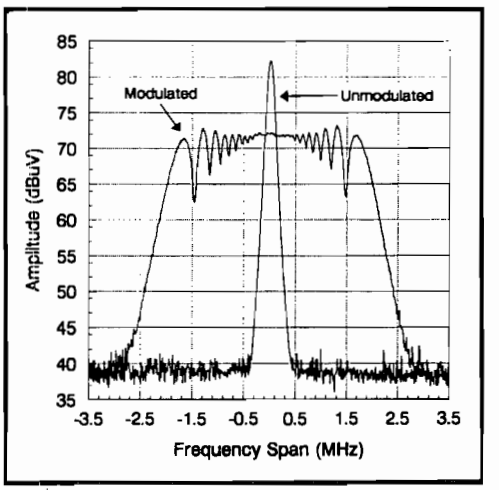

Figure 1. *Measured Frequency Spectrum of a 315-MHz Clock Harmonic With and Without SSCG.*

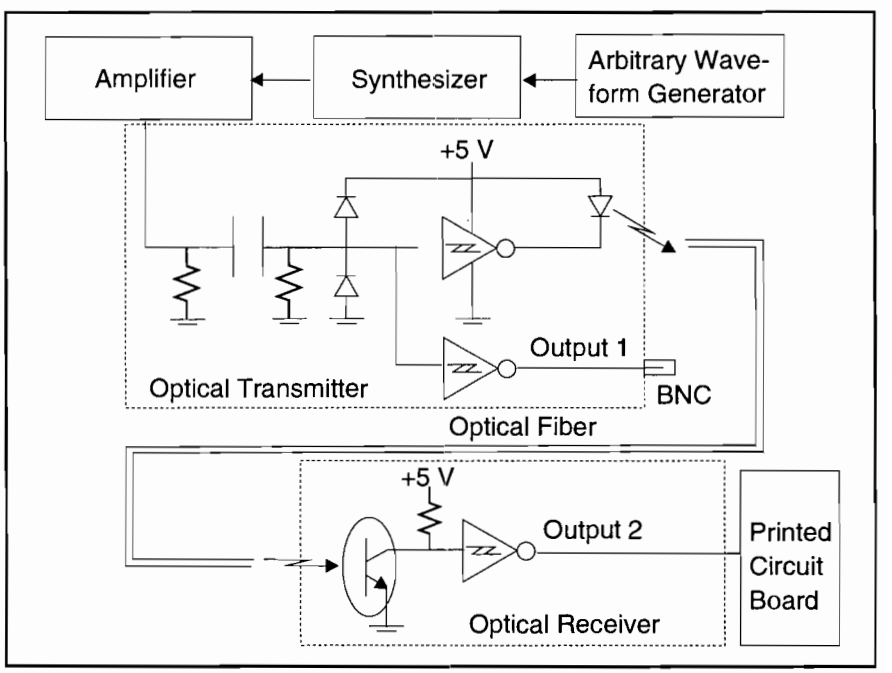

Figure 2. *Experimental Implementation of SSCG.*

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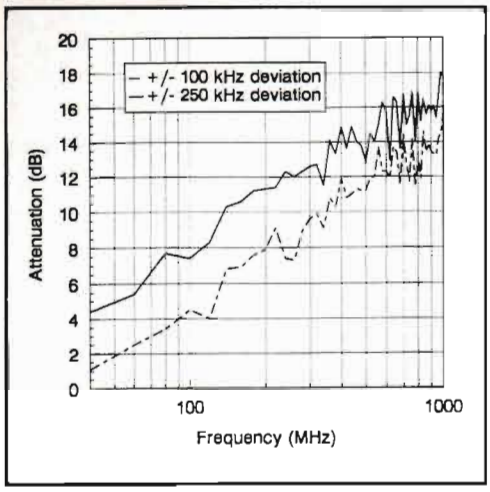

Figure 3. *Measured Attenuation of a 20-MHz Trapezoidal Pulse Train With ±100 kHz and ±250 kHz Deviations.*

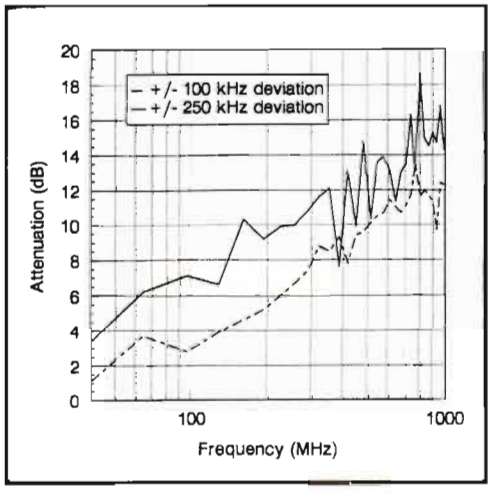

Figure 4. *Measured Attenuation of a 32-MHz Trapezoidal Pulse Train With ±100 kHz and ±250 kHz Deviations.*

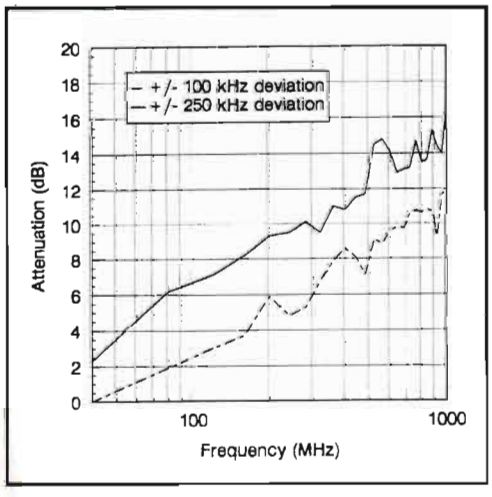

Figure 5. *Measured Attenuation of a 40-MHz Trapezoidal Pulse Train With ±100 kHz and ±250 kHz Deviations.*

the null and changing the amplitude of the Fourier series coefficient by several dB. However, large values of attenuation are not necessary at these frequencies since the amplitudes are at least 10 dB lower than adjacent harmonics.

Prototypes of integrated circuit modules which provide an SSCG clock signal have been evaluated and the results correlate well with experimental data. These dual-inline, small outline integrated circuit (SOIC) packages will replace external crystals or oscillators and will require minimal external components, including a reference crystal.

APPLICATIONS

SSCG has been tested in personal computers and laser printers. Attenuation of the radiated emissions from these products associated with either the clock harmonics or any signals derived from the clock is on the order found in Figures 3 through 5.

Consider the block diagram of a typical personal computer shown in Figure 6. The system can be divided into several subsystems, including the central processing unit (CPU) and math coprocessor, video, I/O controller, hard and floppy drives, and memory. In this system many of the subsystems operate at different fundamental frequencies, with the frequency of the CPU subsystem usually the greatest. Because of this, the CPU and related components often contribute the majority of the radiated emissions of the system. In an example such as this, SSCG could be used to reduce the emissions of the CPU subsystem by providing the fundamental clocking signals for this subsystem. Assuming an SSCG source is used to provide the fundamental clock signal to the CPU, math coprocessor, and cache controller, the emissions of the complete system due to these components could be attenuated as shown in Figures 3 through 5. Obviously, those emissions due to the other components of the system would be unaffected by the introduction of SSCG.

In many cases, subsystems such as those shown in Figure 6 communicate between themselves asynchronously. This asynchronous protocol may allow two subsystems to effectively communicate where one subsystem contains an SSCG source and the other a standard clock source. However, in order for two universal asynchronous receiver transmitters (UART) to communicate in this situation, it may be necessary to limit the peak deviation of the SSCG source to maintain the tolerance required by the receiving UART.

SSCG has additional effects which may limit its usage in some types of electronic products or circuits. For example, in the personal computer shown in Figure 6, SSCG is not used to provide the video clock. Unless the modulating frequency is very high, experimental results have shown that using SSCG in the video circuit results in an obvious wavering in the video display. Any waver detected by the human eye in a video screen is very annoying, so the use of SSCG is not recommended.

CONCLUSIONS

By applying techniques used in communications to intentionally broadband a radio signal, the electromagnetic emissions of an electronic product can be reduced. The primary clock signal in a product is intentionally broadbanded with a unique modulating waveform such that the peak amplitude of the resultant signal, when compared to the unmod-

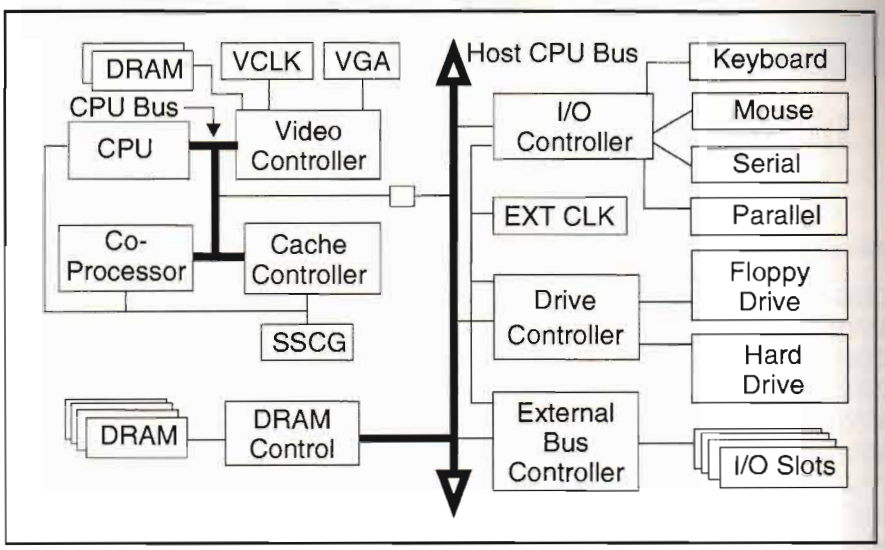

Figure 6. *Block Diagram of an IBM-Compatible Personal Computer with SSCG.*

ulated signal, is significantly reduced. The attenuation provided by the Spread Spectrum Clock Generation, or SSCG, at a given clock harmonic is dependent upon the integer multiplier of the clock fundamental which gives the desired frequency. As the frequency increases, the attenuation also increases due to the increased spreading of the harmonic energy. Measured data demonstrates that attenuation on the order of 10 dB is possible with SSCG.

For those cases where changes in the clock frequency are detectable with undesirable results such as video signals, SSCG may not be a viable solution. However, SSCG may be used in other cases where the peak deviation is limited.

ACKNOWLEDGEMENT

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REFERENCES

1. U.S. Patent pending.
2. K. B. Hardin, J. T. Fessler, D. R. Bush, "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions." Paper submitted to the IEEE 1994 International Symposium on Electromagnetic Compatibility, August 22-26, 1994, Chicago, IL.
3. R. C. Dixon, *Spread Spectrum Systems* (New York: John Wiley & Sons, 1984).
4. H. S. Black, *Modulation Theory* (Princeton: D. Van Nostrand Company, Inc., 1953).

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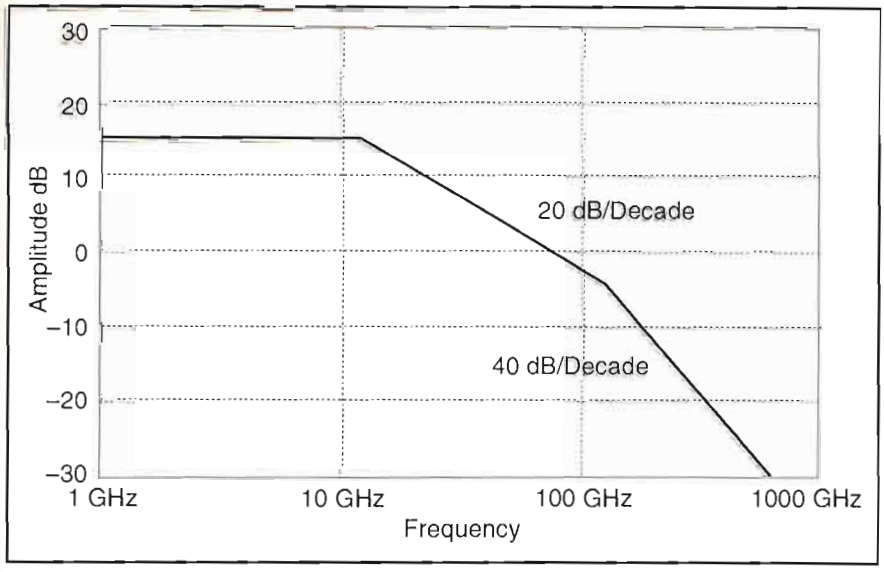

Figure 3. *EMI Amplitude of 15 GHz CMOS Clock with 20 ps Rise Time (Time-to-Frequency Domain Conversion).*

THE PURPOSE OF MOVING FROM ECL TO CMOS TECHNOLOGY

The miniaturization of very large scale integration (VLSI) is limited by the wavelength of the light source used to photographically expose the mask onto the photosensitive coating of the silicon wafer, and by the amount of heat that can be dissipated on the chip to keep the devices at operating temperatures. The etch-resistive coating achieved after developing allows the necessary doping process to fabricate semiconductor transistors, resistors and interconnections of the IC components.

ECL technology is also a lot more expensive than CMOS technology. To proceed with further miniaturization it was necessary to move from ultraviolet (UV) light sources toward shorter wavelength sources such as X-ray lithography. The resulting field effect transistor (FET) MOS technology made it possible to fabricate much smaller MOSFET devices at greater cost savings. The smaller gates on the MOSFET devices have smaller capacitance and allow faster charging, resulting in faster switching. When two complementary transistors, one negative-positive-negative (NPN) and one positive-negative-positive (PNP), are connected in series, only one transistor is conducting at a time. Thus the quiescent current flow present when only a NPN type is used as a switch is eliminated. This allows a reduction of the heat generated with a single transistor switch; much greater density of devices is possible without generating excessive heat dissipation problems.

The actual dc bus is located on the chip surface of the 10^5 to 10^6 CMOS transistors. Their large number results in EMI which is observable in compliance test labs. During switching, a current spike will be impressed on the dc bus. Since most dc buses are metallic conductors of finite length and shape, and carry microwave frequency switching currents, they become unintentional radiating antennas on the chip level and on the PC card level between chips (Figure 4). (A metallic conductor is like an antenna used for radio reception and transmission).

SMALL DC BUSES ON PC CARDS

Simple PC cards are laid out with a minimum of engineering time and expense. Simple electronic devices containing digital ICs mounted on single or doublesided PC cards can be unintentional EMI radiators.[4] Toys, commercial entertainment electronic devices, special function cards for personal computers, and remote radio controllers for various devices are just a few inexpensive products that use simple PC cards. Many of the marketed imported devices do not have the necessary FCC compliance stickers that indicate that they meet Class B device emission standards. Some imported electronic toys from the eastern Pacific countries are good examples.

The electronic devices in use and the type of ICs selected will determine the severity of the problem and the frequency range to be covered. Whether an ECL or CMOS type of device is used makes a big difference. ECL ICs require more current than CMOS devices. Experience shows that the current difference will be made up by the greater density of the CMOS devices, and a less expensive device will encourage designers to use smarter solutions that require more CMOS chips.

The use of one side of a doublesided PC card as a ground plane can reduce the amount of EMI radiated from dc buses. However, cost will be increased because of the increased engineering time needed to work on the ground plane which has to be interrupted where connection feed-through is necessary.

Employing multi-layer PC technology can cure a lot of the problems but it is very expensive. A less expensive solution is to use dc power bus decoupling capacitors on the card. For best results, the frequent placement of a decoupling capacitor for several or even for each HF switching IC is necessary. The decoupling capacitor frequency-impedance characteristics must be selected so that the low impedance covers the frequency spectrum of operation (Figure 5).

Figure 4. *Small dc Bus on a PC Card.*

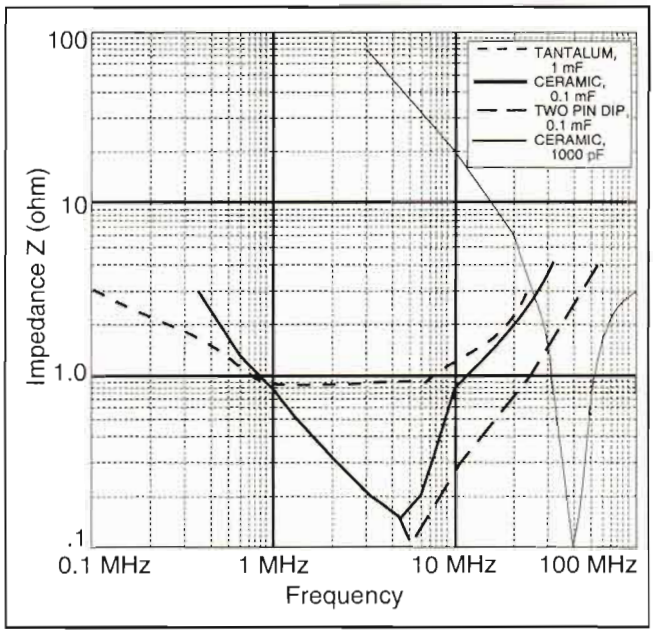

Figure 5. *Frequency-Impedance Characteristics of a Decoupling Capacitor.*

EXAMPLE #1: AN ECL DEVICE

A dc distribution bus on a PC card of 7.5 cm can act as a perfect 1/4 wave antenna at 1 GHz. Given a worst case scenario on a double-sided PC card, and a metallic straight line conductor of 7.5 cm carrying 1 mA of current at 1 GHz in free space, how much EMI will be radiated at a distance of 10 meters?

The electric field for short cable in free space is: [5]

$$E_\theta(V/m) = \frac{(\eta\, I_0 \sin\theta\, dl)}{2r\lambda} \qquad (13)$$

where

η = 377 ohms
I_0 = current in amperes
dl = length in m
r = distance in m
λ = wavelength in m
λ = c/f
c = speed of light in gigameter
f = frequency in GHz

$$E_\theta(V/m) = \frac{(377x0.001x1x0.035)}{(2x10x0.3)} = 0.0047\ V/m \qquad (14)$$

Converting to dBμV/m,

$$E_\theta(dB\mu V/m) = 20 \log (4700/1) = 73.4\ (dB\mu V/m) \qquad (15)$$

Thus, a dc distribution bus carrying 1 mA of current at 1 GHz can radiate as much as 73.4 dBμV/m at a distance of 10 m. A Class B device is limited by FCC regulation to radiate a maximum of 43.3 dBμV/m at a distance of 10 m. As stated, this is a worst case scenario. Since other metallic conductors are always present nearby, the actual radiated emission will be less.

The calculations in all examples are for obtaining an approximation only under worst case conditions. Nearby ground conductors will lower the radiated electric field. For exact solutions an antenna engineering text should be consulted.

EXAMPLE #2: A CMOS DEVICE

A dc distribution bus similar to the one in Example #1 is carrying 100 μA of current (one tenth the current in Example # 1) at 15 GHz. How much EMI is radiated at a distance of 10 meters? The same equation is used as in Example #1.

$$E_\theta(V/m) = \frac{(377x0.0001x1x0.075)}{(2x10x0.02)} = 0.00705\ V/m \qquad (16)$$

$$E_\theta(dB\mu V/m) = 20 \log (7050/1) = 76.9\ (dB\mu V/m) \qquad (17)$$

Thus, carrying 0.1 μA of current at 15 GHz can radiate as much as 76.9 dBμV/m at a distance of 10 m. The allowed EMI limit is the same as in Example #1.

DESIGN COUNTERMEASURES

Observe that in the second example the current flowing in the dc bus is only 1/10 of the current in the first example, but the frequency is 15 times higher. With a ceramic bypass capacitor, the solution is complicated because the frequency impedance characteristics of ceramic capacitors can be low — below 100 MHz — but it is increasingly difficult to find capacitors with low impedance as frequency increases (Figure 5). The new surface mount technology (SMT) capacitors possess better frequency-impedance characteristics. The ultimate solution is for the chip manufacturer to design the decoupling capacitors directly on the chip surface. However, this will decrease silicon yield, and chip manufacturers do not like to decrease silicon yield because of increased cost per device. They would rather let the circuit design engineers cope with EMC/EMI problems.

A laminar bus acts as an efficient, low inductance transmission line (poor antenna) which minimizes EMI radiation (Figure 6).[6] Opposing currents moving in the two conductors reduce the associated magnetic fields to a very low value.

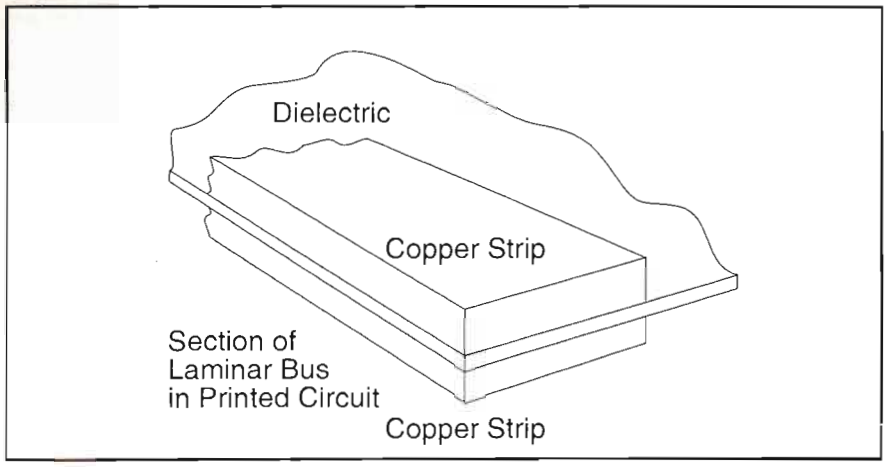

Figure 6. *Laminar DC Bus Design Acts as a Poor Antenna.*

Multi-layer PC card technology allows the designers to lay out the dc bus so that the trace with the dielectric material and the ground plane is an efficient transmission line with the least impedance mismatch. This configuration favors better decoupling of switching transients. Once the dielectric constant and the thickness of the PC glass are known, one is able to calculate how wide a PC trace must be in order to act as an efficient transmission line. The copper thickness determines the current-carrying capacity and the voltage drop. Such a laminar pair of dc buses makes a very poor transmitting antenna and the resulting EMI radiation will be low. Conversely it will make a poor receiving antenna for EMI susceptibility.

MEDIUM-SIZE DC BUS ON PC MOTHER BOARD

When clock cards and data line driver cards are plugged into a PC mother board, the switching currents from the dc bus of the PC card carry high frequency sharp rising pulses onto the PC mother board dc bus. Because of its larger dimensions a dc bus on a large board can radiate more EMI. It also serves as a good receiving antenna for unwanted radiated EMI, distributing it to different cards and input terminals of gates and other components. Interference-capturing electronic devices with ECL circuits has been known to designers for some time. CMOS switching devices can create 100 times more havoc because of their ultrafast rise time and their larger voltage swing. With ECL logic the typical voltage swing is 0.8 volt. With CMOS technology the voltage swing can be as high as 2.5 volt. The current consumption is lower on CMOS devices, but since customers want better and faster performance with more options, the total current consumption is not diminishing; it is growing. Even staggering the switching times cannot lower the total EMI radiated (according to the law of averages).

Decoupling board dc buses from card dc buses seems to help. Multiple plane PC board technology is another solution, but the cost goes up again. The design engineer has to become increasingly aware of EMC/EMI.

MEASUREMENTS OF NEAR FIELD EMI RADIATION

If a spectrum analyzer and a near-field probe is available, it is possible to hold the near-field probe to the PC card or board traces and observe the level of EMI emission during operation. The circuit designer can then try different decoupling capacitors and can observe the magnitude of the radiated EMI signals. The near-field probe measurements will give an indication of the EMI magnitude and an approximation can be made as to how much reduction will be needed to bring the EMI emission down to acceptable levels to meet the requirements of regulatory agencies under a far-field test condition.

Another good use of the near-field probe is to test enclosure EMI leaks and shielding effectiveness. The probe can reveal excessive EMI leakages at cable entrances into the shielded enclosure, and can identify poor door gasket design.

If a LISN (Line Impedance Stabilization Network) is available, the conducted EMI can be measured to determine if it complies with the limits set by the regulatory agencies for conducted EMI.

CONCLUSIONS

The EMC aspects and consequences of the dc bus have been underestimated. Electronic circuit designers become acutely aware of EMI/EMC problems when the electronic product does not pass the regulatory agencies' compliance tests. The traditional and easiest fix is to install decoupling capacitors.

The PC card and PC board designers must develop a greater awareness of how to lay out PC patterns to make the dc bus a laminar transmission line with low EMI radiation. The dc bus must have "bad antenna" characteristics.

PC card/board layout software programs must incorporate EMI/EMC principles to prevent the dc bus from becoming an unintentional radiating/receiving antenna.

Decoupling capacitors with much higher frequency-impedance characteristics will be needed to help reduce EMI in cost-effective products. SMT capacitors cover higher frequency requirements.

The chip designer must become acquainted with all aspects of the new EC Directives since with the ultrafast CMOS devices, decoupling capacitors will have to be "on-chip surface designed" to be more effective. This is possible with six-metal laminar CMOS technology. Better ESD and pulse burst immunity will also result.

To assure that electronic devices can function without interfering with each other, EMC must be designed into each device. Since most electronic devices have dc buses to connect power sources to the electronic circuitry, switching currents, with their high frequency harmonics, are radiated as noise signals from the dc bus. Regardless of how small the equipment is, the length of the dc bus is a finite length, and a finite length of a metallic conductor can act as an unintentional transmitting and receiving antenna. If the interference is strong enough it can interrupt the normal functioning of the electronic device.

REFERENCES

1. Michael Mardiguian, *Interference Control in Computers and Microprocessor-Based Equipment* (1987), p. A.1.
2. Sergei A. Schelkunoff, Herold T. Friis, *Antenna Theory and Practice* (1952), p. 14.
3. William G. Duff, *Fundamentals of Electromagnetic Compatibility*, Vol. 1 (1988), p. 236.
4. Gerald L. Ginsberg, *Printed Circuits Design* (1991), p. 79.
5. William Sinnema, *Electronic Transmission Technology* (1988), p. 264.
6. Frederick W. Grover, *Inductance Calculations* (1946), p. 35.

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RADIATED SUSCEPTIBILITY TESTING USING COMPACT DIAGNOSTIC CHAMBERS *. . . Continued from page 100*

CDC FEATURES	PYRAMIDAL ABSORBER	FERRITE TILES	FERRITE GRID	HYBRID ABSORBER
Outside dimensions (approx.)	7.5 x 5.2 x 3.6 m^3	7.3 x 3.4 x 3.3 m^3	7.3 x 3.4 x 3.3 m^3	7.9 x 4.0 x 3.6 m^3
Inside dimensions (approx.)	6.3 x 4.0 x 2.8 m^3	7.0 x 3.1 x 3.1 m^3	7.0 x 3.1 x 3.1 m^3	7.0 x 3.1 x 3.1 m^3
Applicable specifications	IEC 801-3 and ENV 50140	IEC 801-3 and ENV 50140	IEC 801-3 and ENV 50140	IEC 801-3 and ENV 50140
EMI pre-compliance performance	Poor	Good	Very good	Very good
Nonflammability	Reduced	Very good	Very good	Reduced
Risk of mechanical damage	Tangible	Negligible	Negligible	Tangible
Floor absorbers	Moveable	Fixed	Fixed	Fixed
Frequency range in MHz	80 to >1000	30 to 1000	30 to 2500	30 to 18000
Relative price	1.0	1.4	2.0	2.3

Table 2. *Compact Diagnostic Chambers Compared.*

ponent, there are numerous possible interactions between the EUT and the CDC. Therefore all CDCs have been built based on the same physical facts, but none of them are absolutely identical.

Table 2 shows the most important parameters of the compact diagnostic chamber.

SUMMARY

The compact anechoic chamber is a flexible and cost-effective solution for radiated susceptibility testing. Adaption to the needs of the customer and the equipment under test can be made relatively easily due to the flexibility of the design.

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