DESIGNING TO AVOID STATIC — ESD TESTING OF DIGITAL DEVICES

INTRODUCTION

As the speed and complexity of computers increase, they become more susceptible to noise or destruction due to electrostatic discharge. The results can be devastating. One toy company had produced its entire product line during the humid summer months only to ship them during the Christmas season. As cold fronts moved throughout the country, complaints came in from department stores and customers that the devices were failing. Even a prestigious telephone company reported that its initial field try of a new phone model turned up field failures which were not noticed in the laboratory. In bedroom environments, which contain large amounts of synthetic materials, a discharge to the phone's dial destroyed internal logic. Fortunately for the telephone company, they had detected the problem early and corrected it before the units were mass marketed.

Detecting electrostatic discharge problems early is the subject of this article. While much has been written in the trade press on how to handle integrated circuits to avoid ESD related damage, few articles have concentrated on tests of digital devices at the product level. This article describes how to set up a lab to test products for electrostatic discharge problems and what to do about those problems when they arise.

ELECTROSTATIC THEORY

In order to understand the effect behind the spark, the theory of electrostatics should be reviewed. As a conductive body, humans can acquire and subsequently become a medium for carrying a charge. By shuffling along on the surface of a rug, a human being can acquire a charge by a process known as a triboelectric effect (Fig. 1). Here, two dissimilar materials such as wool in the rug and rubber in the soles of one's shoes can exchange charge causing the person to build up a significant charge. These two separate materials, rubber and wool, have different affinities for electrons; wool gives up its electrons and rubber absorbs an excess. Therefore, when the two are rubbed together, wool acquires a positive charge and rubber a negative charge. Through induction or conduction the negative charge in the sole of the shoes passes through to the human body.

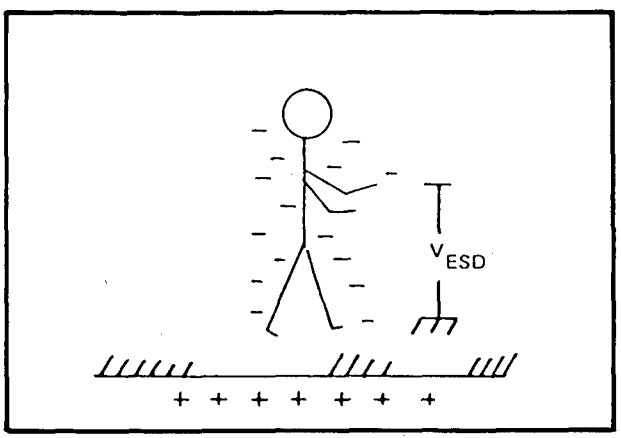

Figure 1. Movement can create a buildup of charge creating a potential (V_{ESD}) for an electrostatic discharge.

Depending on the two materials involved and the rate at which they're rubbed together, two different insulating materials will tend to build up charge at different rates. The affinity for absorbing charge can be ranked in a table and is known as the triboelectric series (Fig. 2). Among the materials which have the greatest affinity for electrons are polyester and teflon. Those that shed electrons easiest include nylon and human hair.

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Sample Triboelectric Series

Positive	Air
	Human Hands
	Asbestos
	Rabbit Fur
	Glass
	Mica
	Human Hair
	Nylon
	Wool
	Fur
	Lead
	Silk
	Aluminum
	Paper
	Cotton
	Steel
	Wood
	Amber
	Sealing Wax
	Hard Rubber
	Nickel, Copper
	Brass, Silver
	Gold, Platinum
	Sulfur
	Acetate Rayon
	Polyester
	Celluloid
	Orlon
	Polyurethane
	Polyethylene
	Polypropylene
	PVC (Vinyl)
	KEL F
Negative	Silicon
	Teflon

Figure 2. The affinity for acquiring or giving up charge can be ranked in the triboelectric series.

Once the charge begins to build up on a human being due to the triboelectric effect, a second effect begins to take place which bleeds off the charge. Humidity in the air can bleed off the charge that resides in the surface of the skin. This is why dry environments tend to be victim to

more electrostatic discharge effects. The rate of charge build-up on a human being is the same, but the charge that is acquired bleeds off so quickly in a humid environment that no ESD problem is usually noticed.

The triboelectric effect causes charges to be built up on the surface of the skin. The amount of voltage associated with that charge build-up becomes a crucial question because it is the electric field caused by the voltage on the fingertip which produces the spark drawn to a nearby metal object. The ratio of voltage that builds up on a fingertip due to the acquisition of a certain amount of charge is known as the body capacitance according to the general formula for a capacitor.

$$CV = Q \text{ or } C = Q/V$$

In order to understand how a conductive body, like a human being, can act as a capacitor the capacitance of a simpler geometry, that of a metal sphere, will be explored (Figure 3). If a metal sphere having no net imbalance of electrical charge is placed in free space, an electron can be moved without work from infinity to the surface of the sphere, because there is nothing on the sphere to repel it.

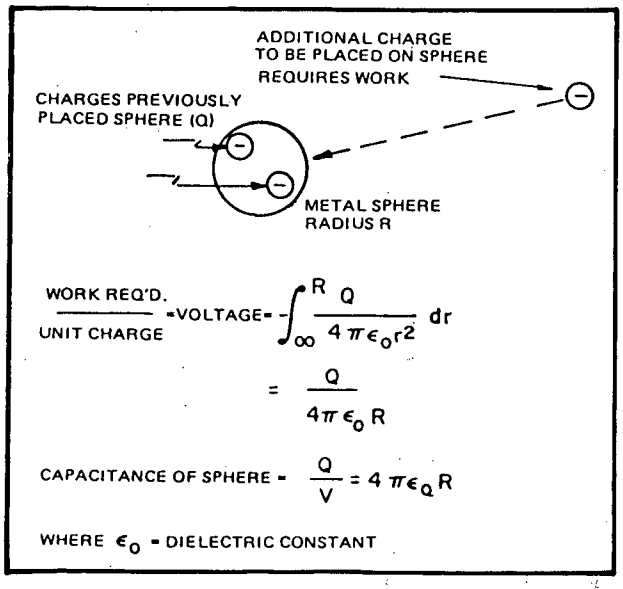

Figure 3. Voltage and capacitance defined. Voltage is the amount of work needed to place additional charge on a metal sphere. The ratio of that charge to the voltage needed to place it on the sphere is the definition of capacitance.

However, work is required to move a second electron from infinity onto the surface of the sphere, due to the repulsion between the second electron and the first. The amount of work it takes can be described by the following formula:

$$\frac{\text{Work Req'd.}}{\text{Unit Charge}} = \text{Voltage} = -\int_{\infty}^{R} \frac{Q}{4\pi\epsilon_0 r^2} dr$$

$$= \frac{Q}{4\pi\epsilon_0 R}$$

where $\frac{Q}{4\pi\epsilon_0 r^2}$ is the electric field at distance r caused by the charge Q already on the sphere. W is the work required per unit charge to move an additional charge on the sphere, and R is the radius of the sphere.

This work is also known by another name. It's called *voltage.*

For small metal spheres, a great deal of work is required to put an extra electron on the surface of the sphere, because the sphere is not large enough to allow the electrons to move very far apart and their repulsive force is strong. For the same reason, large metal spheres take less work or less voltage to apply an extra charge. In fact, the capacitance of a metal sphere is proportional to its radius according to the formula:

$$C \text{ sphere} = \frac{Q}{V} = 4\pi\epsilon_0 R$$

where ϵ_0 is the free space dielectric constant, and R is the radius of the sphere.

Capacitors are often thought of as only two parallel plates. But as this example shows, all conductive bodies have a capacitance of their own without regard to any nearby opposing plate. The parallel plate capacitor is merely one geometry of a capacitor. The human being, like any other conductive body, has a capacitance all its own. The larger the surface area the greater the capacitance.

THE HUMAN ESD MODEL: FIELD STUDIES

In order to establish body capacitance and other electrical characteristics of the human ESD event, numerous studies have taken to the field, measuring actual discharges from human beings in a variety of environments. Typically, these field studies measure (1) the potential build-up on the person prior to discharge (i.e., the open circuit voltage) and (2) how much current results in a discharge to earth ground (i.e., the short circuit current) (Fig. 4). Although some of the parameters associated with human ESD events are still controversial, the studies basically agree on the following.

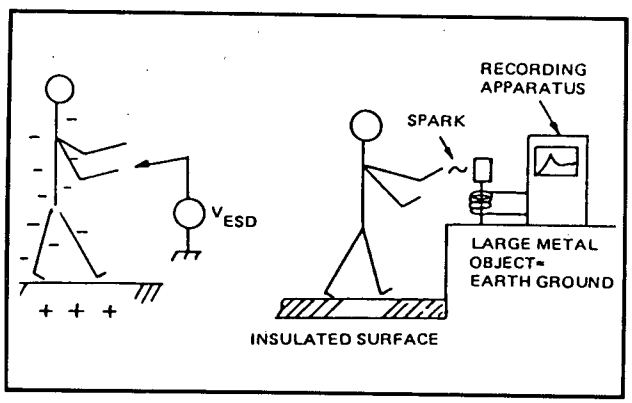

Figure 4. How human ESD models are derived. First, the open circuit voltage on the fingertip is measured. Then the short circuit current is evaluated by discharging to ground and recording the current waveform.

a. The basic human ESD model is a simple RC circuit. Some have proposed using more complicated models (Fig. 5) in order to (1) account for multiple discharges which sometimes occur and (2) create a faster rise time. However, to date, only the simple RC configuration has been widely accepted. At least one international commission, the IEC, has adopted the RC configuration as a standard. Similarly, the Department of Defense, through its MIL Standard MIL-M-38510 has opted for the RC approach.

The simple RC model may in fact be the most accurate. The more complex models have been proposed as mentioned above to simulate multiple discharges and to speed rise time (Fig. 5). Many of the more primitive testers have had trouble achieving the rise time characteristics associated with discharges found in nature and have used speed-up circuits to derive a faster waveform. However, this approach often results in unpredictable ringing and the faster rise

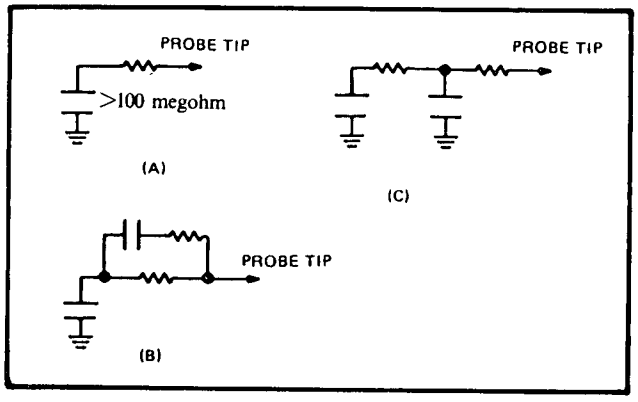

Figure 5. ESD model networks. The simple network (A) is the most widely accepted, and probably best represents an actual ESD event. Figure (B) shows a network with a "Feed Forward" arrangement to yield a faster rise time, but ringing that can result is unpredictable. Two capacitors in Figure (C) attempt to create multiple discharges.

time can be more appropriately achieved by the use of a "charge reservoir" in the front end of the electrostatic discharge generator (see below). To simulate multiple sparking sometimes observed in nature, some of the models employ two capacitors connected together through a series resistor. However, at least one of the studies has indicated that the multiple discharge effect is not common in nature but is actually the result of the hesitancy of test subjects to touch the test apparatus and draw a spark. This hesitancy causes an irregular motion of the fingertip and results in multiple sparking. ESD events which occur in nature don't have this element. The discharge, rather, is a surprise.

b. The most violent discharges occur when a person is holding a metal object. The object "enhances" the electric field causing a faster, higher current discharge. Most ESD models are therefore tailored to the worse case event, a human being holding a pointed metal object. The IEC has adopted a standard for what the probe tip of an ESD simulator should look like.
c. Different ESD events result when a human being is pushing a large metal object such as a cart or a chair against a digital device. Although some commentators have proposed the use of separate networks to model this event, it is considered by many to be such a rare event compared to the normal human ESD discharge that it is often ignored.
d. In nature, both positive and negative polarities can build up on human skin. However, there is no clear evidence that testing with either positive or negative voltage produces different effects. Therefore, most simulators, and standards such as the IEC standard, specify only positive simulator voltages. Furthermore, there is some speculation that high negative potentials can produce free radicals in the air, a potential carcinogen.
e. The worse case waveform observed in nature is that described in Fig. 6. The rise time can be as fast as 1 nanosecond and the current peak as high as 40 amps. Fall time is on the order of 100 nanoseconds.

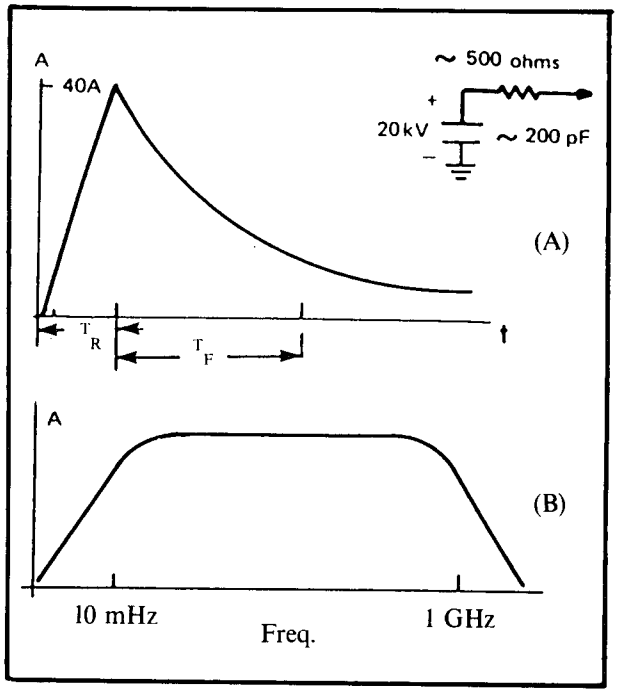

Figure 6. A worst case short circuit current waveform. The peak current is 40 amps, minimum rise-time T_R = 1 nanosecond and maximum fall time is T_F = 100 nanosecond. It can be created by the network shown. Figure 6B is a fourier transform of Figure 6A.

THE HUMAN ESD MODEL: DERIVING THE WORST CASE PARAMETERS

Simple calculations can be used to derive the value of body capacitance (C) and series resistance (R) needed to model the current waveform of Figure 6. The current waveform reaches a peak of 40 amps. Dividing the voltage which produced the waveform by that current yields the minimum series resistance.

$$20kV/40A = 500 \text{ ohm}$$

The maximum fall time from Figure 6 is 100 n sec. The time constant, RC, then yields a value for the body capacitance C

$$RC = 10^{-7}$$

$$C = 200 \text{ pF}$$

The rise time is largely a function of lead inductance and minimizing this lead inductance is a major problem for designers of electrostatic discharge generators (see below). Neglecting this lead inductance for the moment, a worse case model for the human ESD event can be drawn (Figure 6). Using similar calculations, the IEC has adopted a standard consisting of a capacitance of 150 picofarad and a surge resistance of 150 ohms. Many commercial designs in the United States use 150 pF capacitance and a series resistance of 500 ohms.

Because of the fast rise time of the ESD wave form, an ESD event produces high frequency signals. The Fourier transform of the curve is shown in Figure 6. The worse case current wave form produces signals from 10 megahertz to 1 GHz.

SIMULATING THE HUMAN ESD EVENT

Considering that the human ESD model is so simple, it would seem to be a straightforward matter to build an ESD simulator. One would really need only a high voltage power supply, a capacitor, and a surge resistor. However, in practice, serious problems have developed with simple ESD generators which have caused wide variability in test results. One study showed that the use of two different ESD generators caused significantly different test results when used on the same computer. An ESD generator with a fast rise time caused a computer to fail when its output voltage was set to only 4,000 volts. A second ESD generator did not cause the equipment to fail even when a 25 kilovolt spark was applied. (Such sparks can jump a gap of more than a third of an inch.) The second generator differed from the first in one striking parameter: its rise time was much slower.

It is the lead inductance which limits the rise time produced by an ESD simulator, and this lead inductance is extremely difficult to avoid. This lead inductance results not only from the lead length between the discharge capacitor and the device under test, but from the length of the supply return to earth ground as well (see Figure 7). To the first approximation, even very low gauge wires can be modeled as inductors having an inductance of approximately 500 nanohenries per foot. The total amount of inductance in series with the discharge circuit is the total lead length from the device under test through the earth ground return and back to the simulator, a length which

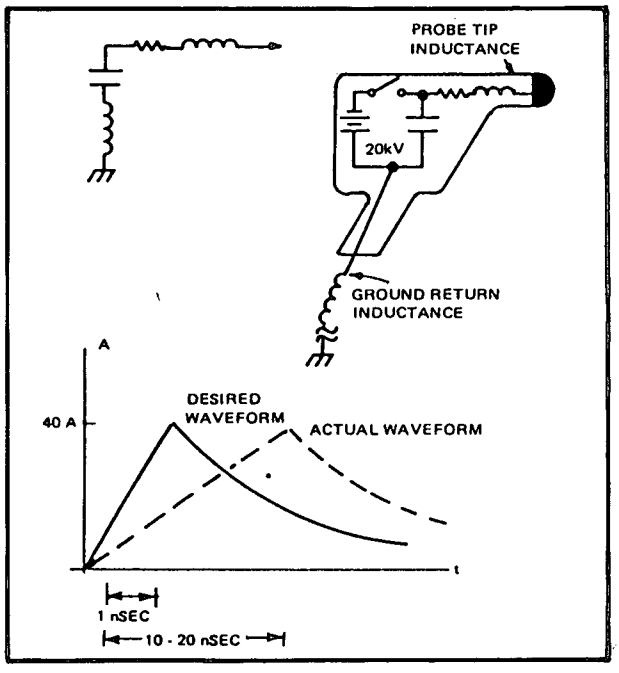

Figure 7. Stray inductance can severely impair the performance of an ESD simulator slowing rise time.

can be on the order of ten feet or more.

In order to understand how lead length affects the rise time, it is helpful to consider the nature of what is commonly called "earth ground." The earth itself is a very large, more or less conductive sphere and has an enormous capacitance derived in the same way that the capacitance of the sphere in Figure 3 was derived. No matter how much charge is placed on the earth or how much current is passed through it, its voltage relative to the rest of the universe does not change very much. Because of this effect, the earth is called a "ground." A "ground" is a point whose potential does not change measurably with man-made currents passing through it. It is always at the reference potential (zero volts). When the capacitor in Figure 7 is charged to 20 kilovolts, the potential across it remains until a spark is drawn. Once current begins to flow, it flows up through the ground return lead which, as mentioned, is inductive. The total amount of current that is drawn instantaneously is a function of the impedance due to this inductance plus the series resistance. Therefore, what primarily limits the rise time is the inductance of the ground return. For most configurations the rise time is therefore highly unpredictable since it is a function of the total ground return length. The total ground length is the total distance from the ground side of the capacitor, through the line cord, through the house wiring, and eventually to the earth itself. Furthermore, at very high frequencies the ground return impedance becomes complex and the rise time becomes slow, difficult to predict, and the wave form produced tends to ring severely.

One way to shorten the ground return path is to ground the ESD simulator to the case of the device under test. In

this way, return currents flow directly through a shortened return path (Fig. 8). Unfortunately, this set up is considered by many to be inadvisable. In a natural discharge, a human being acts as a capacitor, discharging accumulated charge into a digital device. This device's potential relative to earth ground then rises and the amount of the voltage rise depends on its physical size (i.e., its capacitance). Eventually this voltage will bleed off through the earth ground return. If an ESD simulator with its ground return path attached to the chassis is used, the ensuing current flow will be completely different from what would occur in nature. Rather than the current returning through the ac third wire ground return path, it returns through a shortened path to the simulator causing different and unpredictable effects. In any event, even this relatively shortened ground return path can have significant inductance.

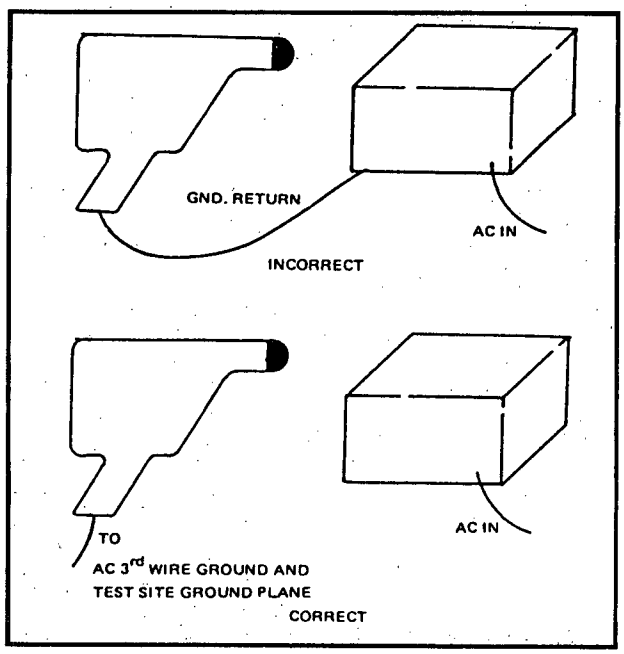

Figure 8. Grounding the ESD simulator to the device under test produces an unnatural current path. The simulator should have its own, independent ground return.

A better way to achieve the fast rise time is shown in Fig. 9. Here two capacitors are used to store charge. One of them is a conventional parallel plate capacitor. Here again current will have to flow up through the earth ground return and through this capacitor when discharge occurs. But the second capacitor is not a parallel plate capacitor. Rather, it's a metallic charge reservoir which works on the same principle as the spherical metal shell in Figure 3. It has a significant free-space capacitance and because it does not use parallel plates to produce capacitance, its discharge rate is not limited by the impedance of the ground return. As soon as the spark is formed the charge will rush off this metal "charge reservoir" giving an extremely fast rise time. Because it operates on the same principle as the human body itself, the resulting ESD event is very similar to the events observed in nature.

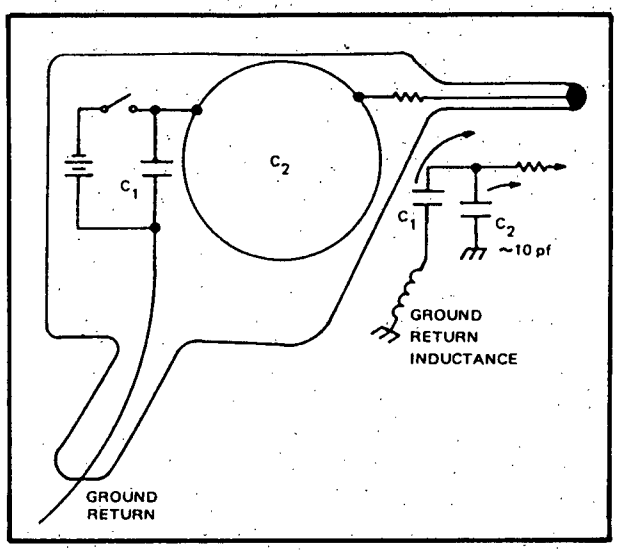

Figure 9. Very fast, consistent rise times are produced by the use of a charge reservoir in the simulator. It acts as a capacitor, but without any ground return inductance.

Most ESD simulators develop a voltage at their tip. The tip is then moved close to the device under test until a spark is formed. Some have proposed designs which place the probe tip directly against the surface of the device under the test. A current is then developed in the device under test by switching over the capacitor to the probe tip. In one design the current passes directly from the capacitor through the surge resistance to the device under test. In another, the current is sent through a small spark gap internal to the unit (Figure 10). Others claim that these designs suffer from drawbacks. First, although they attempt to remove variability from the test procedure by placing the probe tip directly against the surface of the

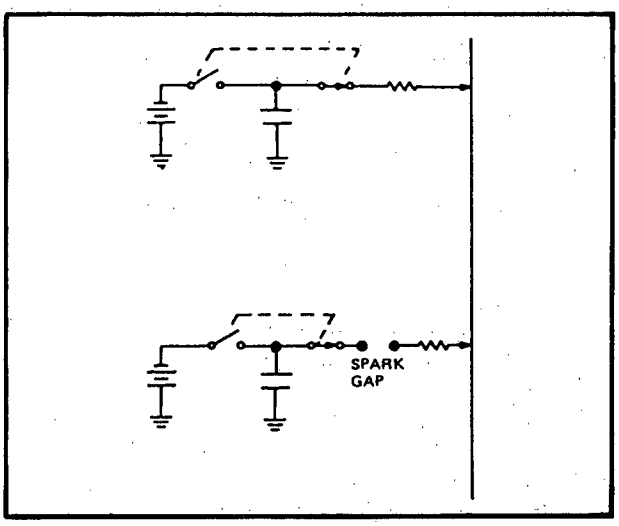

Figure 10. Some ESD simulators apply the probe tip directly against the surface of equipment under test, then charge and discharge the capacitor. However, those techniques have not been widely accepted since it removes an important element of good ESD simulation—the actual spark that occurs.

equipment under test, they do so by removing perhaps the most important physical element of the discharge, the spark itself. The effect of the spark on the waveform produced can be important and methods which test ESD susceptibility without producing the spark on the surface of the equipment raise theoretical questions regarding their applicability. Second, the switching element used to charge the capacitor and then to discharge it can also arc, creating unpredictable effects within the discharge generator itself. Because of these effects, most producers of ESD simulators still recommend charging the probe tip, then bringing the probe tip close to the equipment under test drawing a visible arc.

SETTING UP A TEST SITE

In setting up a test site the temperature and the humidity do not need to be controlled. While low humidity is required for human beings to build up high voltages, the high voltage supply built into a properly designed ESD simulator supplies the proper potential regardless of the humidity level. However, a test site must have one parameter controlled. It must have a reference earth ground available (Figure 11). Since the effect of an electrostatic charge is due to a potential difference between the probe tip and earth ground, a good earth ground which will not vary in voltage when a discharge occurs is necessary. If the voltage varies, then the instantaneous amount of current flowing from the probe tip and through the device under test would be reduced and the worst case waveform shown in Figure 6 could not be achieved.

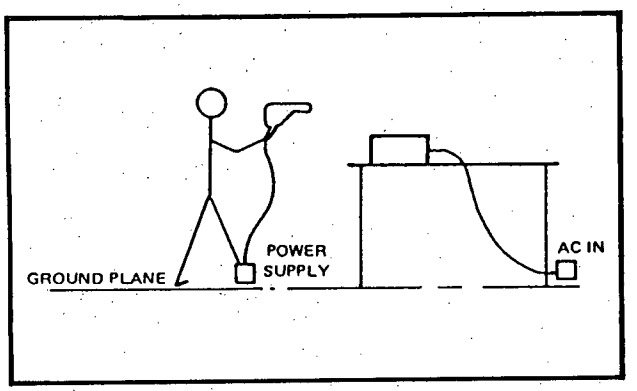

Figure 11. A ground plane is needed on the floor of the test site in order to supply a local earth ground.

However, creating a reference ground encompasses some of the same difficulties described above. The third wire return cannot be used alone because it is inductive and knowing how much inductive path exists between the test site and earth ground via the laboratory's ac wiring is impossible. Therefore, a local "earth" ground must be created. This can be accomplished by the use of a large ground plate.

A ground plane on the floor of the test laboratory should be created whose potential will not charge very much during discharge. This ground plane is a metallic object which, like a metal sphere, has a free space capacitance all its own. Empirical studies have placed this capacitance at about 30 pF per square foot. Therefore, a 20 foot x 20 foot ground plane "looks" like a very high quality 12,000 pF capacitor. Note that proximity to another plate is not needed to derive this capacitance. Energy is stored in the field proximate to the plate itself, not in the dielectric between one plate and an opposing plate.

Since the discharge capacitor is 150 picofarad or so, the capacitance of the ground plan system should be many times that amount. A ground plane approximately 20 feet on a side has a capacitance of 12,000 pF. Even if the ESD generator was discharged directly to a ground plane or this size, the voltage of the ground plane would rise only slightly. By attaching the ground plane to the third wire return, this voltage can be bled off into the earth ground. For safety considerations it's important that the ground plane be attached to the third wire ground in the laboratory's electrical system.

Once the ground plane has been established, the facilities must be arranged to simulate as closely as possible the kind of environments encountered in the field. In practice, floor standing units may be in contact with the metal floor or they may be standing on an insulated surface. Because of this, floor standing devices should be tested in two ways; first, sitting directly on the ground plane and second, insulated from the ground plane with a spacer. Fig. 12 shows this arrangement.

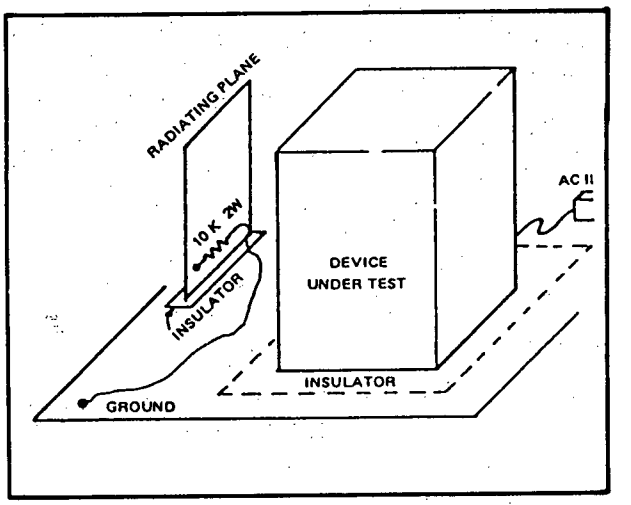

Figure 12. For floor standing units, tests should be run with the device under test both (1) standing in contact with the metal plane, and (2) with an insulating layer approximately ½" thick. The "radiating plane" useful for indirect discharges, can be moved around the device under test.

Similarly, desk top units may be used on a metal or an insulated table. Because many of the components of destructive electrostatic discharge are radiated electric fields, nearby metal objects, such as the surface of a metal table, can change test results by changing the incident field on the device under test. Therefore, both configurations should be used (Fig. 13). Once again it is important to ground the metal desk to the ground plane in order to prevent the build-up of a potentially harmful charge on the surface of the desk.

A third feature of the site is simply a metal plane which can be moved around the device under test. This allows a simulated discharge to a nearby object as opposed to the device under test itself. In cases of severe ESD susceptibility, discharges even to a nearby metal object will cause the equipment to crash. Discharging to this "radiating plane" first may help to illustrate an ESD problem without directly discharging to the unit itself. Units which are extremely susceptible are often destroyed by a direct discharge.

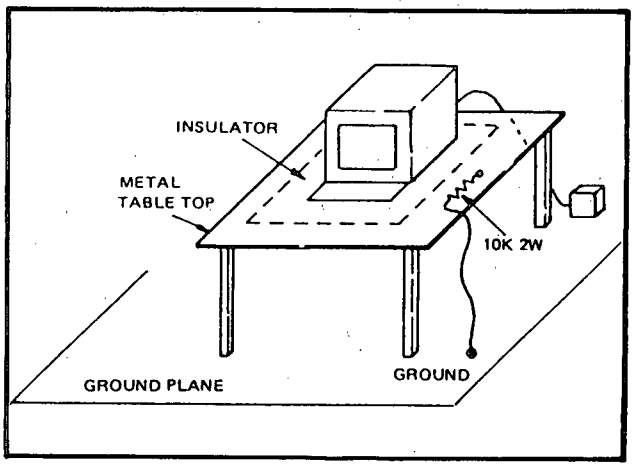

Figure 13. For table top units, testing should be done with and without the insulating spacer. A metal table top should be used, grounded through a 10K resistor.

Two other features of the test set-up must be considered before testing proceeds. First, the software used to exercise equipment under test should be software which queries all the devices on the microcomputer's bus including I/O and all memory locations. In this way, ESD problems which may be associated with a particular port or memory location will show up during testing. Any output device should display the results of the interrogation of each port and each location of memory in such a way as to be able to detect a change in state of a I/O pin or memory location which may be inadvertently ignored by a simpler test program. Secondly, because many of the disruptive effects of electrostatic discharge are caused by radiated emissions, cables should be attached to at least one port of each kind on the equipment under test. These cables can act as antennas, picking up the radiated emissions and passing them down the cable, where they may be interpreted as data. During testing, cables should be moved in every configuration likely to be encountered by the end user in order to determine which particular configuration enhances the likelihood of error. Ideally, these cables should be terminated with a peripheral which has been previously checked for ESD problems. If the peripheral is not available, the cables can be left unterminated. However, the I/O should be strobed periodically to detect the presence of false data caused by the discharge.

With these arrangements in place the testing can begin by setting the ESD simulator to a low starting voltage such as 5 kilovolts. The first discharge should be made to a nearby object, such as the "radiating plane." By moving the plane around the equipment under test, problems can be found with poorly designed units. The voltage should be increased in 5 kilovolt steps to 20 kilovolts. Approximately 20 discharges at each voltage level is sufficient for this phase of the test.

If discharges to the radiating plane do not reveal ESD problems, a preliminary phase of testing can begin by discharging to the device itself. This will determine at what points the equipment under test is most susceptible, and what arrangement of I/O cables and peripherals results in the most system upset. Every point likely to be touched by the end user should be probed, starting with a low voltage such as 5 kilovolts. Special attention should be made to the face of a CRT, keyboard and connector back shells since these are frequently touched. During this phase of the testing, cabling should be moved and the placement of any peripherals varied to find the positioning which causes the most errors. The operator should note what points on the equipment under test are most susceptible and what placement of cables and peripherals causes the greatest system upset.

Once the preliminary scan has determined the location of greatest sensitivity and worst case cable and peripheral placement, a more detailed examination of these spots can be made. Discharging to each of these sensitive locations at least 50 times at a low voltage such as 5 kilovolts is the first step. This is followed by increasing the voltage in 5 kilovolt steps up to 20 kilovolts and observing how many system errors are caused. If an acceptable number of system errors is produced during the 50 discharge test, the operator should move on to other points on the equipment under test and repeat the examination. All in all, a good electrostatic discharge test takes approximately two to four hours to complete.

CRITERIA FOR PASSING AND FAILING

System upset can occur in three basic forms. First there are *transient* system upsets which do not permanently alter the system operation. These include snow or roll of a video screen or a momentary slowdown of printer operation. A second kind of error is more serious. *Soft errors* come in two forms. Some are *correctable* and the operator can correct the problem with a keyboard entry. Others are *non-correctable* and the operator cannot undo the damage without re-initialization. Finally there are *hard errors* which are defined as equipment destruction. For all systems these are intolerable.

A company can choose its own criteria for how many transient, soft errors and hard errors it will allow. However, the standard listed in Figure 14 is representative of that accepted by many companies. At 5 kV no transient errors, soft errors or hard errors are tolerated. At 10 kilovolts, 50% transient errors are tolerated, 5% correctable soft errors but no non-correctable soft errors or hard errors. At 15 kilovolts there is no specification for transient errors. Correctable soft errors are limited to 15% and non-correctable soft errors to 5%. Once again, no hard errors are tolerated. At 20 kilovolts there is no specification for transient or soft errors. However, tests up to 20 kilovolts should be run to determine vulnerability to hard errors.

A word of caution. Normally, the amount of energy stored by the capacitor in the ESD simulator is not high

enough to hurt anyone seriously. It can, however, cause a discomforting shock and serve as a surprise to the unwary. Because of this, care should be taken when using any ESD generator. The equipment under test and any metal objects to which discharge could occur must have a third wire safety ground. Care should be taken at all times to observe the placement of the discharge probe's tip to make sure that unintentional discharge does not occur. Needless to say, those with medical problems, especially cardiac problems, should not be involved with ESD testing.

Test Voltage	Transient Errors	Soft Errors		Hard Errors
		Correctable	Non-Correctable	
5kV	0%	0%	0%	0%
10kV	50%	5%	0%	0%
15kV	100%	15%	5%	0%
20kV	100%	100%	100%	0%

Figure 14. A table of tolerable errors. The table indicates what percentage of errors are tolerable at different discharge voltages.

CURING ESD SUSCEPTIBILITY

There are two primary causes of ESD susceptibility, *radiated* and *conducted upsets. Radiated upset* occurs when an ESD event hits a metal object causing near field electronic disturbances. These are picked up by sensitive components on the equipment under test and read as signals. In the case of *conducted upset*, the arc jumps onto the printed circuit board itself and current passes through traces on the PC board or components causing false data, or in extreme cases, damage to the components themselves.

The cure for radiated upset is easiest to understand if discussed in terms of a discharge to a nearby metal object and not to the device under test (Fig. 15). This, for example, occurs when the test simulator is discharged into the radiating plane as described above. An electric field is created and this field is transmitted into the device under test. If the shielding is inadequate, cables or traces on the PC board can act as antennas, picking up the emissions and coupling them into the components. If they are strong enough, they can be interpreted as signals causing disrupted operation. Because interface cables are the longest antennas attached to a device under test, they act as very good sources for picking up these emissions. They couple the signals that they pick up into the I/O ports where they can be interpreted as data.

The cures for this kind of upset are straightforward. Shielding, or enclosing the entire printed circuit board in a metal shell, can reduce the effect of radiated upsets on the components themselves. Similarly, an I/O cable can be shielded and as long as that shield has a properly designed boot (a 360 metal shell as opposed to a pigtail) connected directly to a metal chassis, good shielding suppression will result. As an alternative, I/O inputs can be bypassed with a small bypass capacitor on the order of 470 picofarads. This bypass capacitor, however, has to be connected to a good ground which means the chassis, not signal ground. In severe cases a pi filter can be used instead of a bypass capacitor.

Radiated upset can also occur when the discharge is to be the shield of the device under test itself. If the shield is a six-sided completely sealed metal box, no amount of current passed through the shield would cause radiated upset to occur inside and no disruption to the electronic circuitry would result. However, discontinuities in the shield, such as cracks, apertures, and seams, cause RF voltages to build up on the shield. This RF causes electric fields to occur internal to the shield which affect the functioning of the logic. In a sense, it is the shield which now acts as a radiating plane and can excite the I/O cables or internal wiring causing false data. Furthermore, bypass capacitors may be of limited effectiveness or even harmful

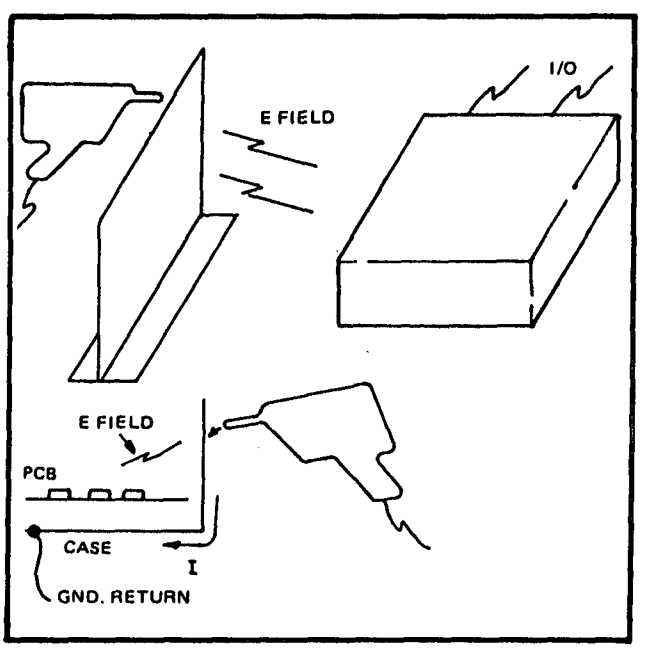

Figure 15. Radiated upset can result from discharges to nearby metal objects or to the device under test itself. Currents flowing through the metal create R F voltages and E fields, which can be picked up by wires acting as antennas and interpreted as false signals.

if the shield does not have good integrity. If currents in the shield can build up significant RF potentials, these potentials can be coupled into the I/O inputs through the bypass capacitors.

There are two approaches to solving radiated upset caused by the excitement of a device's shield by an electrostatic discharge pulse. The first approach is simply to make the overall as complete as possible. By making the shield a nearly seamless six-sided box, internal fields can be reduced or eliminated. A continuous metal shield will not have RF voltages dropped across it, will function well as a shield, and will allow bypass capacitors to become effective.

Conducted upset arises when the current finds its way to the PC board and then passes through either the traces on the PC board or through logic itself (Fig. 16). This causes disruption to the operation of a device. In severe cases, damage to the components themselves can result. Usually, the cure for this problem is simply to insulate areas of the PC board with a plastic or nonconductive compound to prevent the spark from jumping onto the PC board itself. Grounding exposed metal parts to the third wire ground return can also help to make sure that potentials don't build up on these exposed parts, which can subsequently cause a second arc to occur between these parts and the PC board.

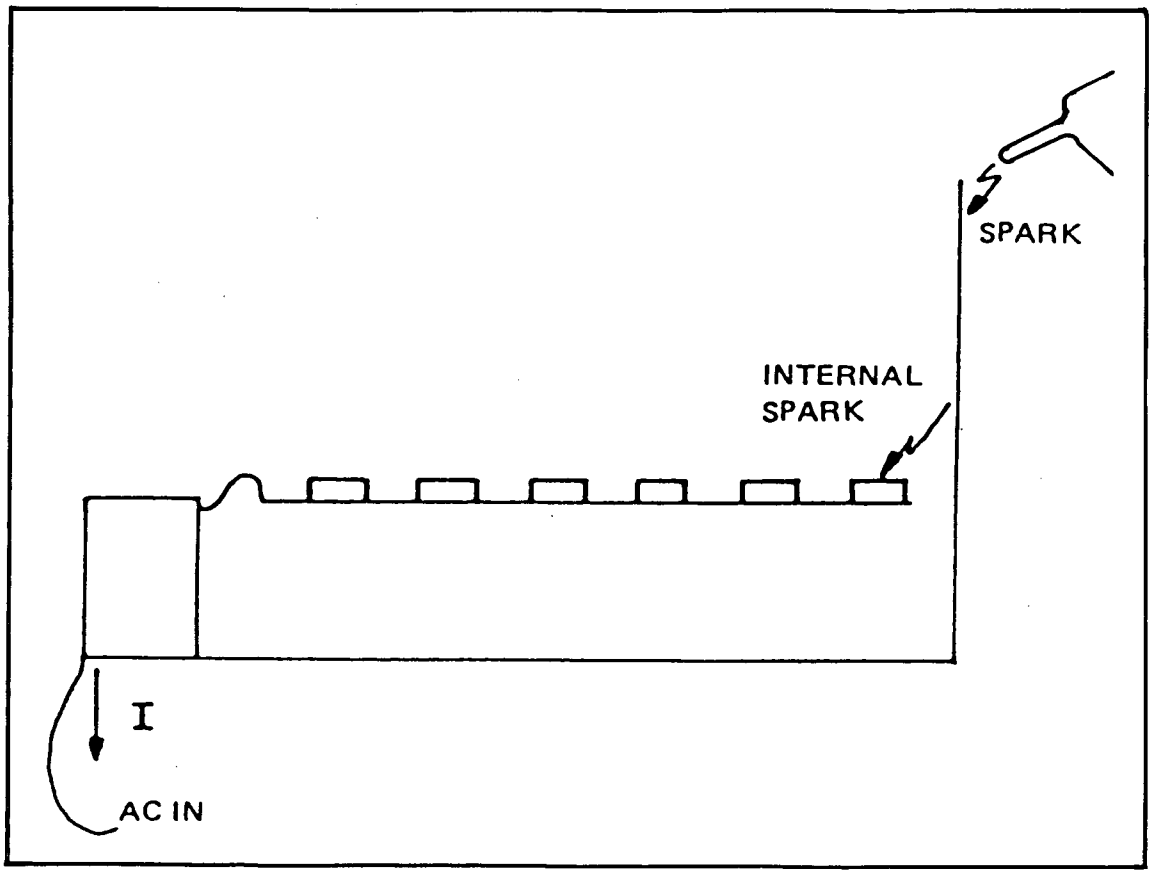

Figure 16. In conducted upset discharge jumps onto the PC board itself returning through the power supply. It can cause false data or destroy parts.

For cosmetic reasons, it may now be possible to make a metal housing of the unit with enough electrical integrity to eliminate ESD problems. In this case, a second approach can be used. Here a second internal shield is employed over the PC board. Bypass capacitors bypassing input lines are grounded to the second shield. The second shield is connected to the first shield at the point where electrical power enters the unit. In this way the outside shield acts as a radiating plane producing fields in its interior. However, the second shield which does not have RF current flowing through it provides the additional shielding necessary for suppression. Often a ground plane under the PC board, or a multilayer board with a buried ground layer can achieve a similar effect.

Finally, the role of properly designed software in eliminating ESD problems should not be overlooked. Error recovery software can often be a substantial help in avoiding annoying soft errors. Also the design of I/O ports can be chosen to limit susceptibility to ESD. Inputs should not be edge triggered (i.e., designed to capture the leading edge of input wave forms). These inputs will be quite susceptible to registering false signals when an ESD event occurs. Rather, inputs should be latched by a strobe which makes coincidence between the strobe and the ESD event necessary for a false indication to be recorded.

This article was written for ITEM 85 *by Glen R. Dash, Dash, Straus & Goodhue, Inc., Boxboro, MA.*

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