EMI/EMC ASPECTS OF HIGH-SPEED INTERCONNECTING NETWORKS & PACKAGING: CROSS-TALK & COMPROMISING EMANATIONS

Smaller and denser integrated circuits and packages need improved interconnection designs to achieve an optimal trade-off between electrical performance/inherent EMI/EMC and scaling-down strategies. Specifically EMC compliance vis-a-vis self-generated cross-talk in the system interior and compromising emanations (information-bearing signals) detectable at the system exterior need specific design considerations.

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HIGH-SPEED DIGITAL SYSTEMS

Self-generated electromagnetic interference plagues modern digital systems which employ fast-switching devices assembled in dense packages with concatenated networks of parallel or nonparallel interconnecting-lines. The resulting cross-talk between the neighboring lines induces false-switching and consequent logic-upsets. Further, the high-speed switching signals may induce conductive and/or radiative compromising emanations which can be detected by clandestine eavesdropping receivers and used to gather classified/security information. Main-frame computers, large telecommunication switches, automatic test equipment, etc. are often confronted with this system-generated problem; and scaling-down strategies designed to fit devices within a specified space aggravate this problem because of the increased proximity of the interconnects.

In high-performance/high-speed digital systems, the rise-time of the signals involved are in the nanosecond/subnanosecond regions with the corresponding bandwidths extending up to gigahertz range in frequency. Thus in terms of signal transmission, the interconnects of high-speed digital systems can be regarded as high-frequency transmission lines. Hence, the signal propagation in the chip-to-chip communication is essentially governed by the interconnect-line parameters, namely, the characteristic impedance (Z_0), line-length and terminal impedances. Accordingly, the integrity of the digital waveform is controlled by the propagation delay and reflections at the interconnect end-points. The proximity/density of the interconnects determines the extent of mutual coupling which may cause the inter-line-interference or "cross-talk". To minimize the effects of self-generated EMI in high-speed digital systems, the interconnect designs must control impedance(s) appropriately. This method is known as the controlled impedance approach. Further, the impedance mismatch will cause EM energy leakage via radiative and/or conductive processes; and these emanations, if they could be detected or received in the system exteriors, would constitute problems regarding TEMPEST.

Since high-speed switching signals have broad spectral characteristics, the entire system is an environment in which electromagnetic emissions may proliferate. Therefore, design studies of interconnections and circuit-packaging are important in achieving the required electromagnetic compatibility (EMC) for complying with the various regulatory specifications of government and/or industry (e.g., NASCIM 5100A, MIL-STD 461).

HIGH-SPEED INTERCONNECTING NETWORKS AND PACKAGES

High-speed digital ICs are difficult to analyze because of their complexity. The maze of wiring and the inherent three-dimensional nature of the circuit cannot be characterized as a simple electromagnetic boundary value problem. Partly for this reason and partly because there appear to be some inherent limitations to the speed range of these circuits (due to skin effects), a full wave analysis is not often necessary. Analysis using lump coupled elements and/or distributed parameter calculations with subsequent transmission-line analysis is usually satisfactory.

The most obvious design requirement of superfast digital systems is to achieve reliable circuits with better density and higher speed. These requirements can be translated into specific electrical design protocols as indicated below and detailed in Figure 1:

- All signals on the system must meet timing requirements. A corollary is that the path lengths should be minimized and the longest critical path identified.
- The signal waveshapes must be within a given tolerance. For example, a negative transition may lead to additional switching delay.
- Unwanted signal coupling between wires must be less than an upper bound so that coupled signals (cross-talk) do not cause improper switching of the logic circuits.
- Voltage transients on voltage dis-

tribution wires (and ground) induced by switching circuits must be limited to small fractions of the dc levels.

- External electromagnetic disturbances should not cause false switching of the digital cirucuits (EMC compliance).

In the last decade an important shift has taken place in the design of high-speed digital hardware with the advent of smaller and denser ICs and packages. Previously, the hardware components consisted of both physically and electrically large discrete parts. Usually stray elements and coupling among the components were limited, and the interconnections between the components were electrically insignificant. The corresponding electrical network models were highly decoupled, and the network analysis matrices sparse. This design lent itself to relatively simple analysis models. In contrast, today's high-level of integration leads to very large and complex systems with extremely small physical dimensions. Therefore, an electrical analysis that excludes coupling among the closely-spaced components is inadequate. Also the interconnections that once led to insignificant stray elements are now the main parts in the equivalent circuits. Thus, the circuit models for IC systems are extremely complex with highly coupled hardwares. An electrical analysis of these models without computer-aided design techniques is not possible especially for high performance systems.

The type of hardware designs which lend themselves to minaturization are microwave, digital- and analog-type systems. Usually, the overall dimensions of the relevant parts of a subsystem for which a signal for coupling analysis is of interest are less than a few centimeters. Often, the highest frequency component in the signals propagating in the system corresponds to a wavelength (which exceeds the physical and electrical dimensions in many cases) and makes the analysis with lumped-circuit models valid.

The type of analysis required for a particular system depends on its performance and purpose. The electrical analysis may be a very simple one for low speed or low frequency circuits since the reactance of the capacitance is high and the inductances are almost short-circuits. A simple analysis with a few LCR elements may be sufficent. In contrast, complex models are required to represent high speed/high performance systems. The signal transitions in very low speed systems may be in the micro- or even millisecond range. At the other end of the system, one is concerned with the analysis of a Josephson or MESFET technology where the signal transitions are in the picosecond range.

A fundamental quantity which characterizes a particular interconnection technology is known as the general impedance level. It is simply the lossless characteristic impedance (Z_0) of the "average" connection in the system. Typical values of Z_0 range from 5 to 200 ohms. In lower performance FET logic hardware, the devices are typically of a higher impedance than Z_0, and thus the capacitance is the dominant circuit element. Bipolar transistor logic hardware may exhibit impedances of the order of Z_0, so that both capacitance and the inductance are important. Josephson junctions exhibit a very low internal impedance, and the inductance is regarded as the dominant stray element.

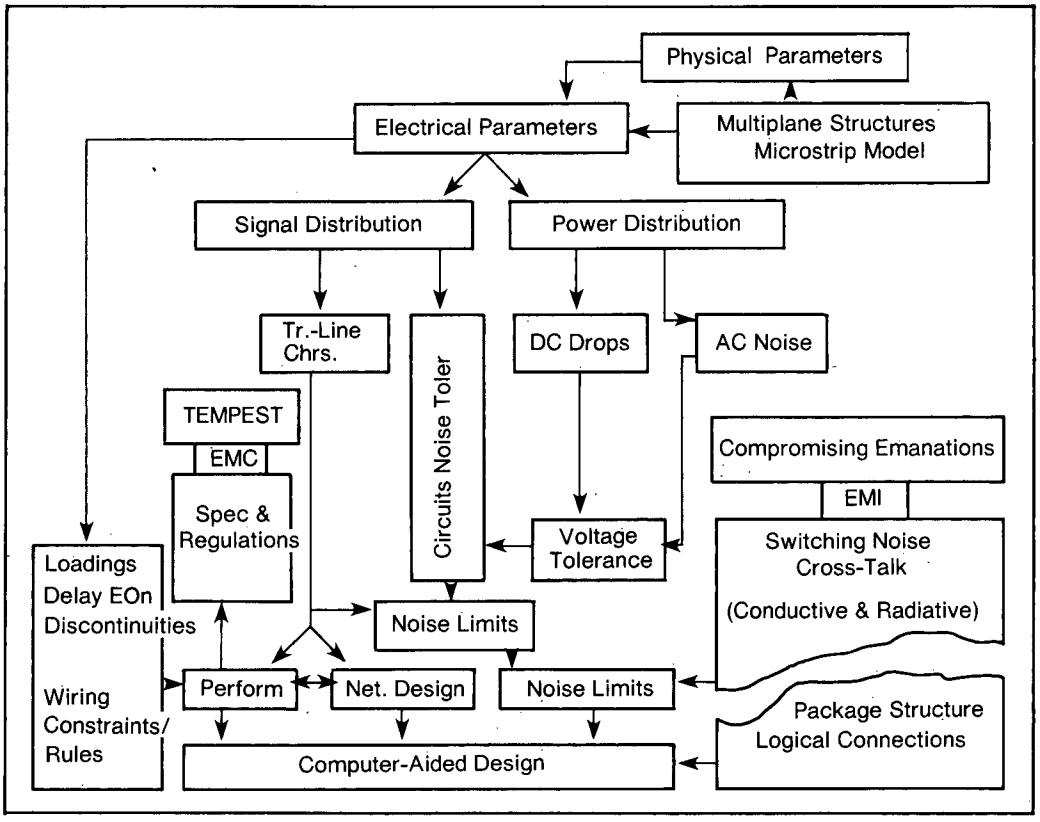


Figure 1. CAD Flow-Chart For Package Design.

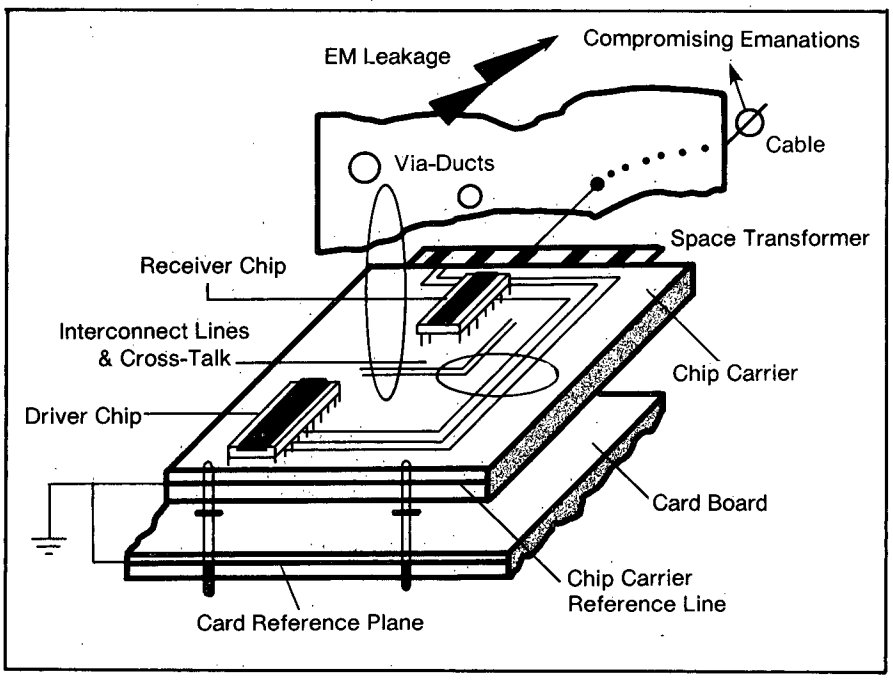


Figure 2. Package-Environment For Chip-To-Chip Communication.

COMPUTER-AIDED DESIGN APPROACH

The computer-aided electrical analysis of interconnections suggested here is based on computational electromagnetics and RF transmission-line theory. The steps involved in the modeling are:

- Preliminary/Approximate Model: The unknowns are expressed in terms of voltage and current using the circuit theory concept.
- Lumped Element Model: RLC representation of the transmission line and computation of the circuit elements.
- Analysis of the modeled circuits to evaluate their electrical performance.

Integrated circuits chips are placed on a chip carrier (Figure 2) which is sometimes called a space transformer since it transforms the closely spaced IC chip connections to larger connection points. The connections among the chip carriers are established in the multiplane board. A logic signal may start with an LSI circuit located on one chip and may be received by a circuit located in the other chip. Thus, the signal may be delayed by both the integrated circuits and the package. In lower-performance systems delay is usually caused by the circuits while package delay is common with high performance hardware. Thus, the purpose of computer-aided electrical analysis is to ensure that the hardware at hand meets the electrical design criteria. The analysis of digital system interconnections encompasses a wide spectrum of frequencies. Therefore, a mixture of static, quasi-static and dynamic models is employed in high-speed digital systems. Quasi-static models such as lumped equivalent circuits play an important role in the representation of the complex physical geometries. Further, an analysis with an inexhaustive model may lead to valuable information without solving the complete dynamic problem. One example is the analysis of a low impedance voltage supply system with an inductance-resistance model. On the other hand, a complex capacitance-resistance model may suffice to represent most parts of a low current, high impedance FET package.

In the above-mentioned modeling approach(es), three specific computational algorithms are possible. The first is an analytical method, the second method uses numerical techniques, and the third approach is based on analog simulations (Figure 3).

Analytical methods (including empirical formulations) provide the fastest solutions but are limited currently to simple geometries. By proper hybridization with numerical and/or empirical approaches, "quasi-analytical" methods can be evolved. Depending on the size of the problems (as decided by the number of unknowns/discrete elements), CAD will lead to solutions with acceptable error limits.

Pure numerical solutions are quite popular in the existing research, design and development efforts. Integral equation methods[1] to calculate two-dimensional circuit parameters of transmission-lines have been successfully developed. However, the major problem with this method is that the state-of the-art computers severely limit the calculations to about 100 elements before unacceptable errors are noticed. Further, computational process time increases enormously when the size of the matrix formulation increases to accommodate more unknowns. Although improved computational algorithms based on conjugate gradient technique, method of moment, etc. have been evolved to handle large-sized problems[2], computational limits persist. The trade-offs between accuracy of analysis and the size of the problem are depicted in Figure 3.

Another problem associated with packaging/interconnections is the propagation of pulses on transmission-lines. Examples of propagation problems for chip-to-chip communication and multi-chip interconnection lines and cross-talks are illustrated in Figure 2. Two problems which have impeded further progress in this area of high-speed networks. One is the need for CAD tools for analyzing propagation on lossy coupled nonuniform transmission-lines with nonlinear sources and loads. The other is the challange of developing CAD tools for analyzing cross-talk parallel and nonparallel transmission lines and multiple reflection phenomena on interconnected transmission lines. In both these cases, the modeling techniques are limited by state-of-the-art computers with their limits in memory and execution time.

To summarize, the following are the imminent needs of high-speed packaging/interconnection systems which can be conveniently and more effectively handled with CAD implementation:

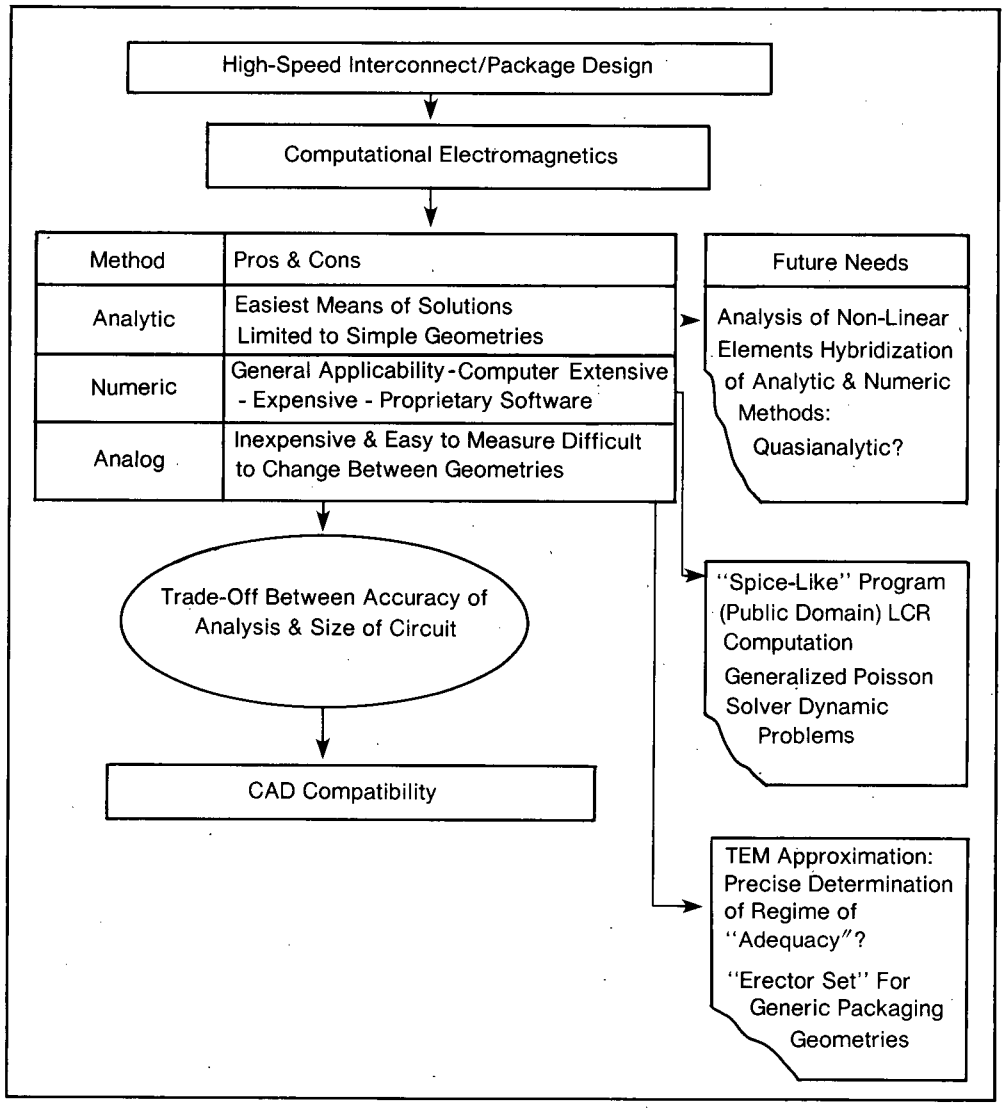


Figure 3. CAD Vis-A-Vis High-Speed Circuit Interconnects.

- Development of automated design tools which incorporate lumped and distributed parameter-based algorithms into transmission-line/circuit analysis leading to CAD programs.
- Development of methods for analyzing steady-state and transient propagation on lossy coupled nonuniform transmission-lines with nonlinear loads and sources.
- Development of methods to analyze coupling between parallel and nonparallel transmission-lines and multiple reflection phenomena on interconnected transmission-lines.
- Development of methods for accurate estimation of the mutual capacitance matrix corresponding to 100 or more metallic elements.
- Development of stable methods to synthesize equivalent circuit models of complex package structures using measured frequency domain data. Relevant results will be used to analyze packages in the time domain.
- Studies on the limits of applicability of various design-methods for lumped and distributed parameters and the extendability of CAD strategies.
- Stochastical characterization of pulse propagation on transmission-lines which are effectively nonuniform with a "random" constant because they pass through a complex changing environment.

HIGH-DENSITY MULTIPLANE PACKAGING: STRIPLINE MODEL

Stripline structures with multiconductor transmission-lines embedded in multielectric media (Figure 4) simulate the multiplane high-speed digital systems. Existing design-algorithms for these are based on conformal mapping techniques, Green's function formulation, variational method, Fourier transform approach, Fourier integral solution (Figure 5) and generalized spectral-domain analysis. Compatible with futuristic broadband/subnanosecond operations, relevant analysis should also consider the lossy behavior of the stripline structure. Thus the algorithm will refer to a dynamic problem involving Green's function solution[3]

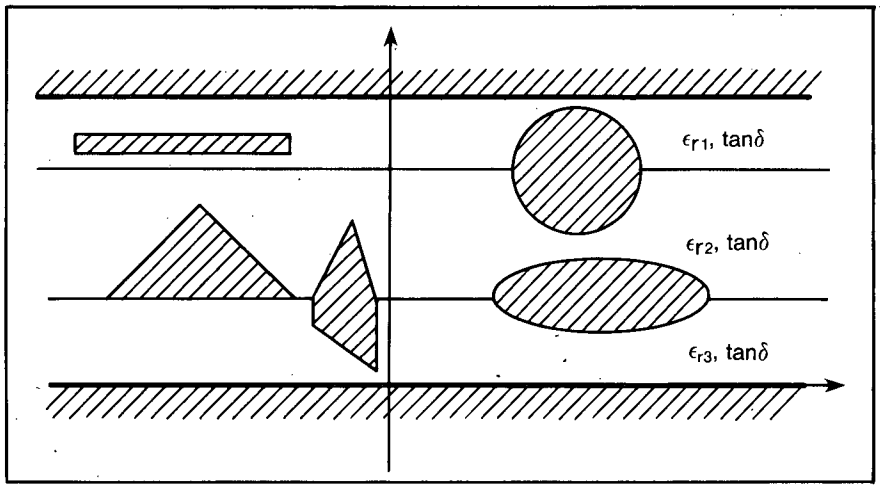


Figure 4. Arbitrarily-Shaped Multiple Conductors in Multilayer Lossy Dielectrics: A Generalized Microstrip-Line Model.

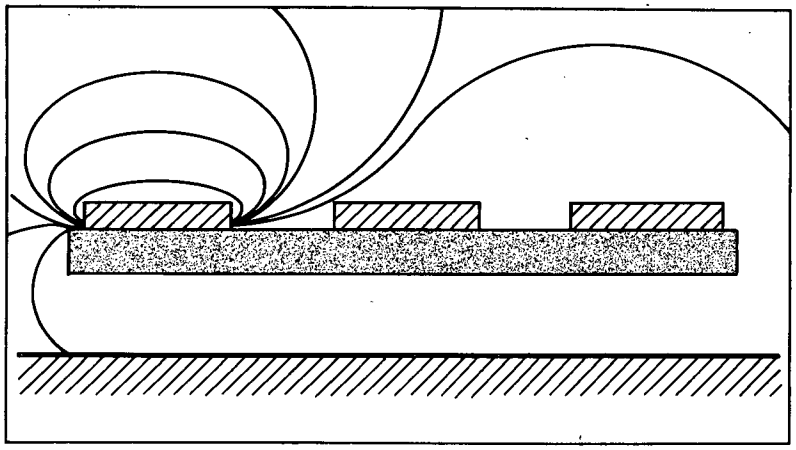
with a scattering matrix solvable by the method of moments[2].

The numerical design approach of this problem will require the conversion of an operator equation to a matrix equation for necessary solution. However, the matrix involved will depict such a large system of equations that use of the state-of-the-art CADS will not suffice. Therefore, a new algorithmic approach (such as the conjugate gradient method[2]) to solve the nonself-adjoint operator equation iteratively has been evolved. Relevant to this area, specific problems which can be addressed via CAD strategies are as follows:

1. There are a very few numerical methods currently available for adequate characterization of junctions and bends in transmission-lines carrying high-speed digital signals (with frequency spectrum extending into several GHz). What is needed is a full wave solution for analyzing microstriplines[4] and efficient ways to compute[5] radiations (emissions) from microstrip structures.
2. As circuits become clustered together, methods should be developed for accurate characterization of proximity effects, parasitic coupling and effects of discontinuities and junctions. Again, emphasis is to be given to full wave solution since radiation/emission is an integral part of the model.
3. There is a need to find the physical limits of a high-Q circuit (depicting low-loss interconnect systems) At most, a quality factor (Q) of 100 is attainable for open resonator structures in planar configurations. The question that is yet to be answered is: What is the ultimate value of Q that is theoretically attainable?
4. What is the typical characteristic impedance one should utilize in the design of interconnecting lines for controlled operations? For example, with a low characteristic impedance line, the circuit is tightly coupled and the losses are high. A high characteristic impedance, on the other hand, indicates that fields are very loosely coupled and that the structure is highly prone to electromagnetic emissions. The key questions are what should be proper characteristic impedance and how should this be based on an optimum external interference criteria and losses in the circuit. Considering the complexity of the problem, the optimum solution can be reached only via CAD.
5. Currently, there is no nonlinear large-signal device model available. Moreover, such a model would be inaccurate if it were based on static/quasistatic data and therefore did not include any high-frequency or dynamic representations. Also, most numerical models tend to ignore the effect of the dielectric substrate for printed circuits and radiation effects. Hence, for accurate modeling of microstrip circuits representing high-speed systems, it is necessary to solve Maxwell's equations with the proper boundary conditions in a more exact fashion.

ELECTROMAGNETIC COMPATIBILITY

Radiation emissions from high-speed signals propagating in the chip-to-chip communication protocols (Fig-



Boundary Element Method Green's Function Solution of Field Problems

$G(r/r') = -\ln|r - r|$ (Green's Function).

$\Phi(r) = \frac{1}{2\pi\epsilon} \int_s \sigma(r')G(r / r')\,ds' + C$ ⟶ Galerican Procedure

Potential ⟷ Charge Distribution

(Integral Equation) ⟶ $S\sigma = b$

(Algebraic Matrix Equation)

Figure 5. Simple Microstrip Structure/Analysis.

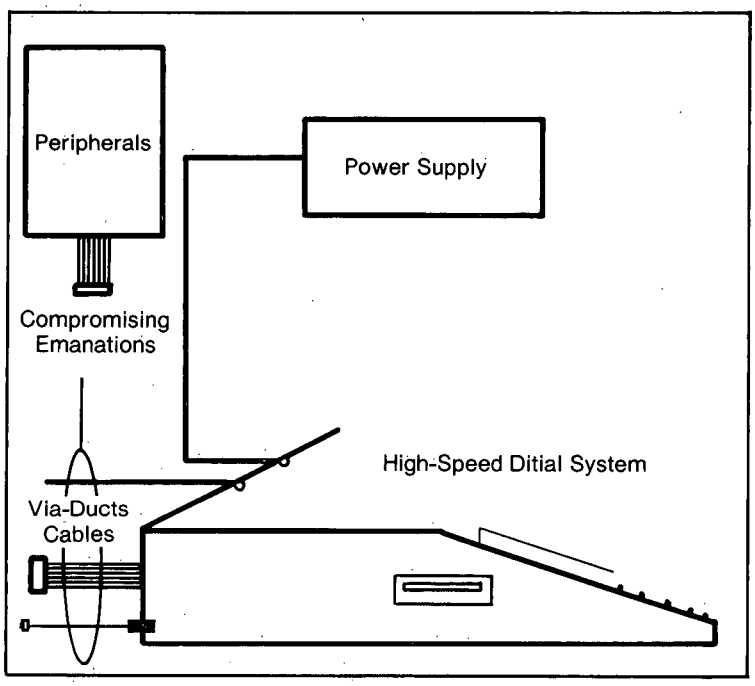


Figure 6. The TEMPEST Environment.

ure 2) warrant EMC compliance of interconnections and circuit packaging. EMC of system-generated electromagnetic pulses is now a design objective in almost all electromagnetic equipment. It derives its original impetus from FCC Docket 20780 and has been suplemented by various DOD/MIL specifications.

For many years, system engineers have tested their finished electronic equipment for EMI and RFI using MIL-STD-461 and 462 which provide adequate guidelines for active systems. However, despite the advanced shielding techniques being advocated for optimum EMI-free performance (stipulated by MIL-STD-461 and 462), the problem of self-induced EMI in high-speed digital systems needs further detailed examination in design reviews. The paths through which EMI may reach the other components are the direct interconnecting lines (mutually-coupled) and radiative emissions. Because of these two offending sources of EMI (namely, conductive and radiative), it becomes essential to seek design alternatives which alleviate or eliminate EMI. The possible approaches are shielding, grounding, filtering, circuit-packaging, controlled impedance-based interconnect designs/cables and/or a combination of all of them. Additionally, the chosen approach must be cost-effective.

To study the EMC of a given equipment meeting the Class A and Class B interference limits, the following standards are usually useful:

- FCC Docket 20780 on permissible conducted interference.
- FCC Docket 80284 on EMI test requirements.
- MIL-STD-462 on EMI characteristics and measurements.
- MIL-STD-461 on EMI characteristics, requirements for equipment.
- MIL-C-85485A on RF absorptive cable, electric filter line.
- DOD-STD-1766 on surface impedance testing of cables.
- MIL-HDBK-235 on classified environments.
- NASCIM 5100A TEMPEST.

Inclusion of EMC compliance in the CAD strategies pertaining to design of high-speed digital systems is appropriately indicated in the flowchart of Figure 1. EMI/EMC control in high-speed digital systems is of great concern in TEMPEST work. Avoidance of compromising emanations (Figure 6) or unintentional information-bearing signals (which could be intercepted and analyzed for classified information) is mandatory; and the package design must comply with the relevant regulatory measures.

CONCLUSIONS

To ensure the design integrity of a high-speed digital system, the future design models should be CAD-based. The CAD formulations should convert the logical data flow decided by EMI/EMC considerations into a set of design-rules for practical implementation. Both EMI and EMC should be taken into the design strategy with exhaustive inclusion of all the package parameters in the areas of signal distribution, EMI/noise sources and power distribution. Microstrip analogy can be effectively utilized for the design methods involved. Basically, reduction of internal cross-talk problems and externally accessible compromising emanations is the core EMC objective in the design of high-speed digital systems. ■

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