# Predicting EMI from DC Buses in Digital Equipment

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## INTRODUCTION

The EMI emission source that most modern digital electronic devices have in common is the direct current (dc) bus that supplies and distributes necessary electric power to integrated circuits (IC).

DC buses are used in almost all digital electronic devices, including satellite transmitters and receivers that enable worldwide communication, earth resources imaging, and collection of navigation and weather forecasting data; and in electronic tools for medical research and care, personal computers, cellular and cordless telephones, and electronic games and toys. The proliferation of these electronic devices is causing a rise in interference between susceptible devices. The dc bus becomes an unintentional radiating antenna when minute residual switching signals are emitted from the ICs. This article will show by mathematical calculations how to predict the amount of EMI a dc bus will radiate.

Regulatory agencies worldwide are setting allowable limits for radiated and conducted EMI emissions and for EMI susceptibility or immunity levels to assure interference-free operation of all existing electronic devices. A prime example is the European Community (EC), which passed an EC Directive, effective in 1992, in an effort to control the problem of EMI. Any product marketed in the EC countries is required to meet strict EC regulations, and to display the CE Mark to indicate conformance.

***Mathematical calculations can be used to predict the EMI radiated by a dc bus.***

## BACKGROUND OF THE DC BUS

Generally, when ICs are used in an Emitter Coupled Logic (ECL) configuration on printed circuit (PC) cards, the PC layout contains a dc bus and signal traces. The dc bus couples unwanted signals to some ICs unless they are decoupled with high frequency bypass capacitors from the bus. This is especially a problem on a card that contains a large number of densely packed ECL ICs driven by a common clock. The simultaneous switching turn-on current at 200 MHz or at a higher rate will induce on the dc bus a considerable current fluctuation at the clock frequency rate. It is not uncommon to have rise and fall times as short as 1 ns and a large harmonic frequency spectrum extending to 1 GHz and beyond.[1]

The emerging ultrahigh speed technology of complementary metal oxide semiconductor (CMOS) devices is extending EMI from dc buses to much higher frequencies. With CMOS devices, designers can achieve much faster solutions with reduced power consumption than with ECL ICs. The disadvantage of CMOS technology is its faster switching, and the dc bus contamination of ultrahigh frequencies is many times worse. The newer CMOS logic devices can be driven at a clock rate of 1.5 GHz. The rise time of such a short pulse can be as short as 75 ps or less.

Rise and fall times of such short duration occupy a very large spectrum of harmonic frequencies. These frequencies extend up into the microwave region. Such high frequencies are very difficult to contain from residual high frequency (HF) currents circulating in dc buses. The result is radiated or conducted EMI.[2] To curb radiated EMI, manufacturers turn to shielding enclosures, which increase the cost of the product.

## EMI PATHS: RADIATED OR CONDUCTED

The power line is a very good conductor of noise. If the device has an adequate line filter installed, the EMI is blocked in while leaving or entering the device. If a device is equipped with a very good line filter but a very poor dc bus it can still cause havoc with radiated EMI. Conversely the device can become a victim of received EMI.

The EMI source needs a path to its victim for interference to occur. The path may be transmitted on metallic conductors, such as cables and power wires, or it may be radiated in the form of electromagnetic waves through the air waves. The dc bus plays a crucial role in coupling EMI from switching solid-state devices to both conducted and radiated paths. Portable battery powered devices operated with a battery charger or battery eliminator are

often not designed for conducted EMI. This is a frequently forgotten point which causes problems later.

## WHAT IS A DC BUS?

A dc bus is a pair of metallic conductors between one power supply and several electronic devices. Sometimes the electronic device requires the connection of power supplies with different voltage and current ratings, which necessitates using more than one pair of metallic conductor dc buses. One of the requirements of a dc bus is a sufficient cross-sectional area of a good conducting metal, such as copper, to deliver the power supply voltage with an acceptable low voltage drop and with minimum temperature rise. If the dc bus has a voltage drop between the minimum and maximum loads which exceeds the manufacturer's recommended levels, the electronic devices may not function as intended, or a malfunction may take place.

Most electronic devices require at least one dc bus and may contain digital electronic circuits for high clock rate switching. Clock rates of 50 MHz and higher will have an alternating current (ac) component riding on top of the dc voltage. The following equations illustrate how to calculate the time-to-frequency domain conversion. A 50-MHz ECL clock with a 2-ns rise and fall time and with an amplitude of 0.8 volt will occupy a frequency domain beyond 50 MHz[3] (Figures 1 and 2).

$$T = \frac{1}{f_0} = \frac{1}{5\times10^7\ \text{Hz}} = 2\times10^{-8}\ \text{sec} \quad (1)$$

$$\tau = \frac{T}{2} - \frac{(\tau_r + \tau_f)}{2} = \frac{2\times10^{-8}}{2} - \frac{(2\times10^{-9} + 2\times10^{-9})}{2} = 8\times10^{-9}\ \text{sec} \quad (2)$$

$$f_0 = \frac{1}{T} = 5\times10^7\ \text{Hz} = 50\ \text{MHz} \quad (3)$$

where

$T$ = clock period
$\tau$ = clock pulse period
$\tau_r$ = rise time
$\tau_f$ = fall time
$f_1$ = frequency of amplitude
$f_0$ = clock frequency amplitude
$f_2$ = frequency of 20 dB/decade change to 40 dB/decade change.

$$f_1 = \frac{1}{\pi\tau} = \frac{1}{\pi 8\times10^{-9}\ \text{sec}} = 3.97\times10^7\ \text{Hz} = 39.7\ \text{MHz} \quad (4)$$

$$f_2 = \frac{1}{\pi\tau_r} = \frac{1}{\pi 2\times10^{-9}\ \text{sec}} = 1.59\times10^8\ \text{Hz} = 159\ \text{MHz} \quad (5)$$

$$\text{duty cycle, } \delta = \frac{\tau}{T} = \frac{8\times10^{-9}}{2\times10^{-8}} = 4\times10^{-1} \quad (6)$$

The amplitude will be obtained as follows:

$$2A\delta(f_1)(\text{dB}) = 20\log 2A\frac{\tau}{T} = 20\log 1.6\times4\times10^{-1} = -3.8\ \text{dB} \quad (7)$$

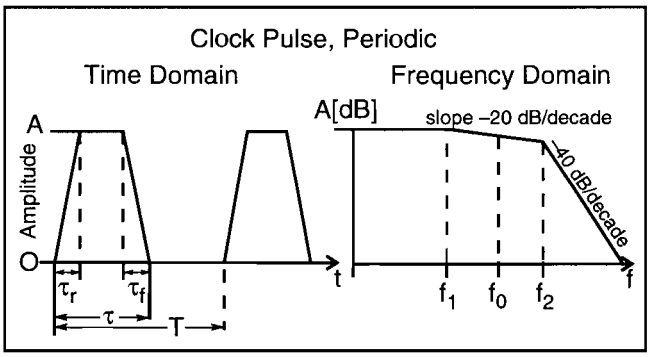


***Figure 1.*** *Time-to-Frequency Domain Conversion of Clock.*

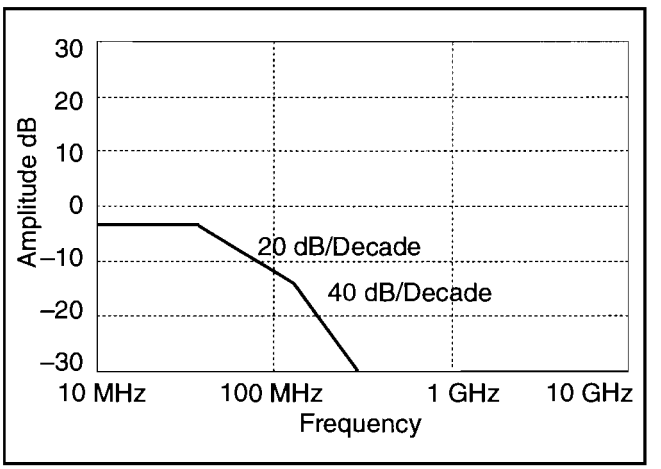


***Figure 2.*** *EMI Amplitude of 50 MHz ECL Clock with 2 ns Rise Time (Time-to-Frequency Domain Conversion).*

$$A(f_0) = 2A\delta - 20\log\frac{f_0}{f_1} = -3.8 - 20\log\frac{5\times10^7}{3.97\times10^7} = -5.8\ \text{dB} \quad (8)$$

$$A(f_2) = 2A\delta - 20\log\frac{f_2}{f_1} = -3.8 - 20\log\frac{1.59\times10^8}{3.97\times10^7} = -15.8\ \text{dB} \quad (9)$$

At $f_1$ the frequency domain envelope is starting a -20 dB/decade slope. At $f_2$ the amplitude slope is changing to -40 dB/decade. To find the amplitude in dBμV, add 120 dB to each dB value. Thus:

$$2A\delta(f_1) = -3.8 + 120 = 116.2\ \text{dB}\mu\text{V} \quad (10)$$

$$A(f_0) = -5.8 + 120 = 114.2\ \text{dB}\mu\text{V} \quad (11)$$

$$A(f_2) = -15.8 + 120 = 104.2\ \text{dB}\mu\text{V} \quad (12)$$

Using the previous procedure for calculation, an ultra-fast CMOS clock at a 15-GHz clock rate with a combined rise and fall time of 20 ps and an amplitude of 2.5 volts would occupy a much larger frequency domain (Figure 3).

*Continued on page 283*

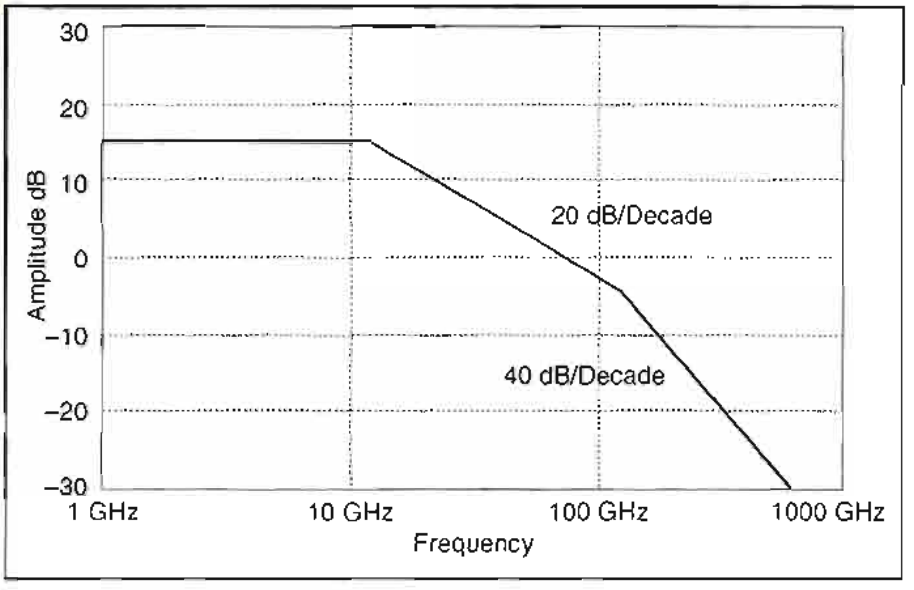


***Figure 3.*** *EMI Amplitude of 15 GHz CMOS Clock with 20 ps Rise Time (Time-to-Frequency Domain Conversion).*

## THE PURPOSE OF MOVING FROM ECL TO CMOS TECHNOLOGY

The miniaturization of very large scale integration (VLSI) is limited by the wavelength of the light source used to photographically expose the mask onto the photosensitive coating of the silicon wafer, and by the amount of heat that can be dissipated on the chip to keep the devices at operating temperatures. The etch-resistive coating achieved after developing allows the necessary doping process to fabricate semiconductor transistors, resistors and interconnections of the IC components.

ECL technology is also a lot more expensive than CMOS technology. To proceed with further miniaturization it was necessary to move from ultraviolet (UV) light sources toward shorter wavelength sources such as X-ray lithography. The resulting field effect transistor (FET) MOS technology made it possible to fabricate much smaller MOSFET devices at greater cost savings. The smaller gates on the MOSFET devices have smaller capacitance and allow faster charging, resulting in faster switching. When two complementary transistors, one negative-positive-negative (NPN) and one positive-negative-positive (PNP), are connected in series, only one transistor is conducting at a time. Thus the quiescent current flow present when only a NPN type is used as a switch is eliminated. This allows a reduction of the heat generated with a single transistor switch; much greater density of devices is possible without generating excessive heat dissipation problems.

The actual dc bus is located on the chip surface of the $10^5$ to $10^6$ CMOS transistors. Their large number results in EMI which is observable in compliance test labs. During switching, a current spike will be impressed on the dc bus. Since most dc buses are metallic conductors of finite length and shape, and carry microwave frequency switching currents, they become unintentional radiating antennas on the chip level and on the PC card level between chips (Figure 4). (A metallic conductor is like an antenna used for radio reception and transmission).

## SMALL DC BUSES ON PC CARDS

Simple PC cards are laid out with a minimum of engineering time and expense. Simple electronic devices containing digital ICs mounted on single or doublesided PC cards can be unintentional EMI radiators.[4] Toys, commercial entertainment electronic devices, special function cards for personal computers, and remote radio controllers for various devices are just a few inexpensive products that use simple PC cards. Many of the marketed imported devices do not have the necessary FCC compliance stickers that indicate that they meet Class B device emission standards. Some imported electronic toys from the eastern Pacific countries are good examples.

The electronic devices in use and the type of ICs selected will determine the severity of the problem and the frequency range to be covered. Whether an ECL or CMOS type of device is used makes a big difference. ECL ICs require more current than CMOS devices. Experience shows that the current difference will be made up by the greater density of the CMOS devices, and a less expensive device will encourage designers to use smarter solutions that require more CMOS chips.

The use of one side of a doublesided PC card as a ground plane can reduce the amount of EMI radiated from dc buses. However, cost will be increased because of the increased engineering time needed to work on the ground plane which has to be interrupted where connection feed-through is necessary.

Employing multi-layer PC technology can cure a lot of the problems but it is very expensive. A less expensive solution is to use dc power bus decoupling capacitors on the card. For best results, the frequent placement of a decoupling capacitor for several or even for each HF switching IC is necessary. The decoupling capacitor frequency-impedance characteristics must be selected so that the low impedance covers the frequency spectrum of operation (Figure 5).

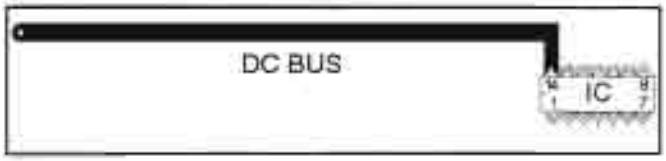


***Figure 4.*** *Small dc Bus on a PC Card.*

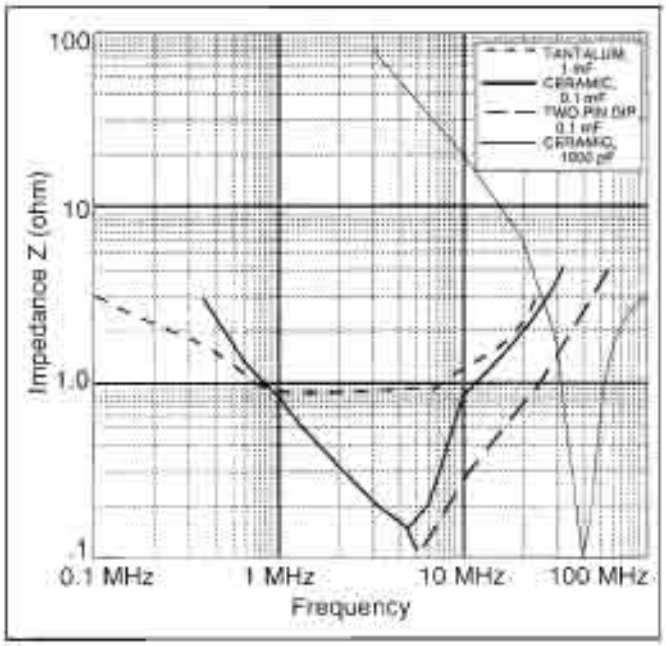


***Figure 5.*** *Frequency-Impedance Characteristics of a Decoupling Capacitor.*

### EXAMPLE #1: AN ECL DEVICE

A dc distribution bus on a PC card of 7.5 cm can act as a perfect 1/4 wave antenna at 1 GHz. Given a worst case scenario on a double-sided PC card, and a metallic straight line conductor of 7.5 cm carrying 1 mA of current at 1 GHz in free space, how much EMI will be radiated at a distance of 10 meters?

The electric field for short cable in free space is: [5]

$$E_\theta(V/m) = \frac{(\eta\, I_0 \sin\theta\, dl)}{2r\lambda} \qquad (13)$$

where

$\eta$ = 377 ohms
$I_0$ = current in amperes
dl = length in m
r = distance in m
$\lambda$ = wavelength in m
$\lambda$ = c/f
c = speed of light in gigameter
f = frequency in GHz

$$E_\theta(V/m) = \frac{(377x0.001x1x0.035)}{(2x10x0.3)} = 0.0047\ V/m \qquad (14)$$

Converting to dBμV/m,

$$E_\theta(dB\mu V/m) = 20 \log (4700/1) = 73.4\ (dB\mu V/m) \qquad (15)$$

Thus, a dc distribution bus carrying 1 mA of current at 1 GHz can radiate as much as 73.4 dBμV/m at a distance of 10 m. A Class B device is limited by FCC regulation to radiate a maximum of 43.3 dBμV/m at a distance of 10 m. As stated, this is a worst case scenario. Since other metallic conductors are always present nearby, the actual radiated emission will be less.

The calculations in all examples are for obtaining an approximation only under worst case conditions. Nearby ground conductors will lower the radiated electric field. For exact solutions an antenna engineering text should be consulted.

### EXAMPLE #2: A CMOS DEVICE

A dc distribution bus similar to the one in Example #1 is carrying 100 μA of current (one tenth the current in Example # 1) at 15 GHz. How much EMI is radiated at a distance of 10 meters? The same equation is used as in Example #1.

$$E_\theta(V/m) = \frac{(377x0.0001x1x0.075)}{(2x10x0.02)} = 0.00705\ V/m \qquad (16)$$

$$E_\theta(dB\mu V/m) = 20 \log (7050/1) = 76.9\ (dB\mu V/m) \qquad (17)$$

Thus, carrying 0.1 μA of current at 15 GHz can radiate as much as 76.9 dBμV/m at a distance of 10 m. The allowed EMI limit is the same as in Example #1.

## DESIGN COUNTERMEASURES

Observe that in the second example the current flowing in the dc bus is only 1/10 of the current in the first example, but the frequency is 15 times higher. With a ceramic bypass capacitor, the solution is complicated because the frequency impedance characteristics of ceramic capacitors can be low — below 100 MHz — but it is increasingly difficult to find capacitors with low impedance as frequency increases (Figure 5). The new surface mount technology (SMT) capacitors possess better frequency-impedance characteristics. The ultimate solution is for the chip manufacturer to design the decoupling capacitors directly on the chip surface. However, this will decrease silicon yield, and chip manufacturers do not like to decrease silicon yield because of increased cost per device. They would rather let the circuit design engineers cope with EMC/EMI problems.

A laminar bus acts as an efficient, low inductance transmission line (poor antenna) which minimizes EMI radiation (Figure 6).[6] Opposing currents moving in the two conductors reduce the associated magnetic fields to a very low value.

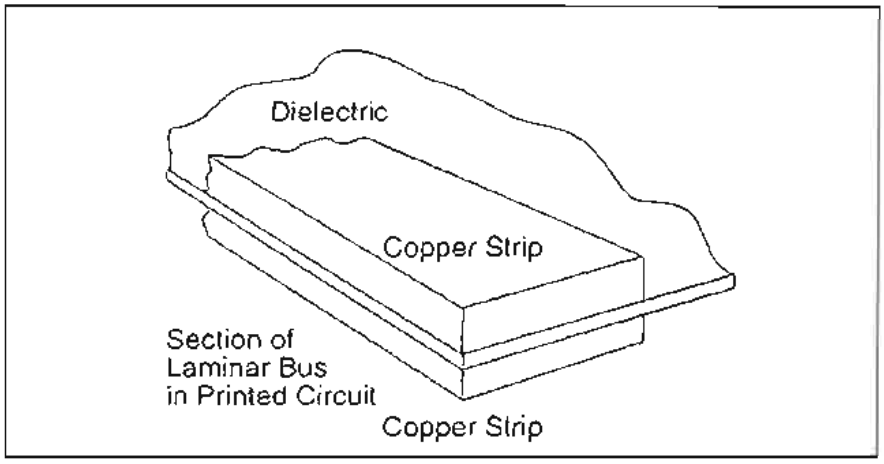


*Figure 6. Laminar DC Bus Design Acts as a Poor Antenna.*

Multi-layer PC card technology allows the designers to lay out the dc bus so that the trace with the dielectric material and the ground plane is an efficient transmission line with the least impedance mismatch. This configuration favors better decoupling of switching transients. Once the dielectric constant and the thickness of the PC glass are known, one is able to calculate how wide a PC trace must be in order to act as an efficient transmission line. The copper thickness determines the current-carrying capacity and the voltage drop. Such a laminar pair of dc buses makes a very poor transmitting antenna and the resulting EMI radiation will be low. Conversely it will make a poor receiving antenna for EMI susceptibility.

## MEDIUM-SIZE DC BUS ON PC MOTHER BOARD

When clock cards and data line driver cards are plugged into a PC mother board, the switching currents from the dc bus of the PC card carry high frequency sharp rising pulses onto the PC mother board dc bus. Because of its larger dimensions a dc bus on a large board can radiate more EMI. It also serves as a good receiving antenna for unwanted radiated EMI, distributing it to different cards and input terminals of gates and other components. Interference-capturing electronic devices with ECL circuits has been known to designers for some time. CMOS switching devices can create 100 times more havoc because of their ultrafast rise time and their larger voltage swing. With ECL logic the typical voltage swing is 0.8 volt. With CMOS technology the voltage swing can be as high as 2.5 volt. The current consumption is lower on CMOS devices, but since customers want better and faster performance with more options, the total current consumption is not diminishing; it is growing. Even staggering the switching times cannot lower the total EMI radiated (according to the law of averages).

Decoupling board dc buses from card dc buses seems to help. Multiple plane PC board technology is another solution, but the cost goes up again. The design engineer has to become increasingly aware of EMC/EMI.

## MEASUREMENTS OF NEAR FIELD EMI RADIATION

If a spectrum analyzer and a near-field probe is available, it is possible to hold the near-field probe to the PC card or board traces and observe the level of EMI emission during operation. The circuit designer can then try different decoupling capacitors and can observe the magnitude of the radiated EMI signals. The near-field probe measurements will give an indication of the EMI magnitude and an approximation can be made as to how much reduction will be needed to bring the EMI emission down to acceptable levels to meet the requirements of regulatory agencies under a far-field test condition.

Another good use of the near-field probe is to test enclosure EMI leaks and shielding effectiveness. The probe can reveal excessive EMI leakages at cable entrances into the shielded enclosure, and can identify poor door gasket design.

If a LISN (Line Impedance Stabilization Network) is available, the conducted EMI can be measured to determine if it complies with the limits set by the regulatory agencies for conducted EMI.

## CONCLUSIONS

The EMC aspects and consequences of the dc bus have been underestimated. Electronic circuit designers become acutely aware of EMI/EMC problems when the electronic product does not pass the regulatory agencies' compliance tests. The traditional and easiest fix is to install decoupling capacitors.

The PC card and PC board designers must develop a greater awareness of how to lay out PC patterns to make the dc bus a laminar transmission line with low EMI radiation. The dc bus must have "bad antenna" characteristics.

PC card/board layout software programs must incorporate EMI/EMC principles to prevent the dc bus from becoming an unintentional radiating/receiving antenna.

Decoupling capacitors with much higher frequency-impedance characteristics will be needed to help reduce EMI in cost-effective products. SMT capacitors cover higher frequency requirements.

The chip designer must become acquainted with all aspects of the new EC Directives since with the ultrafast CMOS devices, decoupling capacitors will have to be "on-chip surface designed" to be more effective. This is possible with six-metal laminar CMOS technology. Better ESD and pulse burst immunity will also result.

To assure that electronic devices can function without interfering with each other, EMC must be designed into each device. Since most electronic devices have dc buses to connect power sources to the electronic circuitry, switching currents, with their high frequency harmonics, are radiated as noise signals from the dc bus. Regardless of how small the equipment is, the length of the dc bus is a finite length, and a finite length of a metallic conductor can act as an unintentional transmitting and receiving antenna. If the interference is strong enough it can interrupt the normal functioning of the electronic device.

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***RADIATED SUSCEPTIBILITY TESTING USING COMPACT DIAGNOSTIC CHAMBERS*** . . . *Continued from page 100*

| CDC FEATURES | PYRAMIDAL ABSORBER | FERRITE TILES | FERRITE GRID | HYBRID ABSORBER |
|---|---|---|---|---|
| Outside dimensions (approx.) | 7.5 x 5.2 x 3.6 $m^3$ | 7.3 x 3.4 x 3.3 $m^3$ | 7.3 x 3.4 x 3.3 $m^3$ | 7.9 x 4.0 x 3.6 $m^3$ |
| Inside dimensions (approx.) | 6.3 x 4.0 x 2.8 $m^3$ | 7.0 x 3.1 x 3.1 $m^3$ | 7.0 x 3.1 x 3.1 $m^3$ | 7.0 x 3.1 x 3.1 $m^3$ |
| Applicable specifications | IEC 801-3 and ENV 50140 | IEC 801-3 and ENV 50140 | IEC 801-3 and ENV 50140 | IEC 801-3 and ENV 50140 |
| EMI pre-compliance performance | Poor | Good | Very good | Very good |
| Nonflammability | Reduced | Very good | Very good | Reduced |
| Risk of mechanical damage | Tangible | Negligible | Negligible | Tangible |
| Floor absorbers | Moveable | Fixed | Fixed | Fixed |
| Frequency range in MHz | 80 to >1000 | 30 to 1000 | 30 to 2500 | 30 to 18000 |
| Relative price | 1.0 | 1.4 | 2.0 | 2.3 |

**Table 2.** *Compact Diagnostic Chambers Compared.*

potent, there are numerous possible interactions between the EUT and the CDC. Therefore all CDCs have been built based on the same physical facts, but none of them are absolutely identical.

Table 2 shows the most important parameters of the compact diagnostic chamber.

## SUMMARY

The compact anechoic chamber is a flexible and cost-effective solution for radiated susceptibility testing. Adaption to the needs of the customer and the equipment under test can be made relatively easily due to the flexibility of the design.


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