Decoupling capacitors as a cause of radiated EMI: an analysis of capacitor placement

Part 2. The Time Domain*

This is Part 2 of a two-part article. Part 1 (ITEM 2000) dealt with frequency domain analysis and effects on how decoupling capacitors can cause radiated EMI. Part 2 examines the time domain of this unique discovery. A small portion of Part 1 is repeated herein to review important aspects of this research.

This article describes design and layout solutions to minimize development and propagation of common-mode RF energy. Included is proper selection and use of decoupling capacitors and how to minimize inductance within a PCB layout. If power and ground planes exist, and proper use of decoupling is implemented, radiated emissions due to use of decoupling capacitors will be minimized.

** Material for this article was extracted from a technical paper presented at the IEEE 1999 International Symposium on Electromagnetic Compatibility in Seattle, WA.[1]*

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SUMMARY OF PART 1 (ITEM 2000)

Development of common-mode radiated energy within a printed circuit board (PCB) occurs because of complex parasitics and layout topologies. When a decoupling capacitor is applied to a PCB for the purpose of reducing or minimizing RF switching noise injected into the power and ground distribution system, interesting results can occur. Radiated emissions may be created and propagated into free space if selection and implementation of the decoupling capacitor is not performed correctly. The key word here is "implemented."

Decoupling capacitors are, however, a primary cause of EMI for PCBs that do not contain power and ground planes. Single- and double-sided assemblies are still being designed and built in ever increasing numbers. This article addresses these design issues. The same effect will be observed on multilayer boards if not laid out correctly.

For different package configurations, except ball grid arrays (BGAs), flip chips, and other configurations that secure a silicon die directly to a substrate without lead bond wires, results of this research applies. Lead bond wires and the routed trace between a discrete component (the capacitor) and the pins of a digital device (power and/or ground) contain inductance. When inductance is present, a voltage drop occurs within the network. This voltage gradient between capacitor and component develops common-mode RF energy. Decoupling capacitors that are supposed to minimize development of RF energy and to ensure signal integrity, may actually be one source of radiated EMI in addition to the common-mode current that exist, within a silicon substrate.

When routed traces are incorporated between capacitor and component, the inductance present allows a dipole antenna configuration to exist. This dipole antenna will efficiently radiate common-mode RF energy within the network. The efficiency of the loop area as a field propagator is extremely poor. Most microstrip loop area dimensions on typical PCBs are resonant in the low to mid-GHz range, yet significant amounts of low frequency (30–400 MHz) energy are radiated and propagated. Under this situation, how is common-mode RF energy propagated if a poor antenna structure exists?

Traces by themselves cannot radiate without a dielectric medium to transfer

an electromagnetic field from a driven element to a 0V-return (ground). A decoupling capacitor establishes a dielectric path that closes the RF propagating loop, thus allowing an electromagnetic field to propagate common-mode energy between the two elements of the dipole antenna. This energy is now observed as EMI.

The dielectric composition (material) of the capacitor emulates free space dielectric by allowing a closed-loop circuit to be present. RF energy in a driven element propagates through the capacitor, allowing this dipole antenna to radiate common-mode RF as a result of poor decoupling implementation, including all switching noise developed internal to digital devices transitioning logic states.

A simplified configuration of the test PCB is shown in Figure 1. Detail on the test setup and complete topology is provided in Part 1 of this article.

The total inductance of a decoupling loop includes the trace length from the power pin of the component to the capacitor, and trace length from the ground terminal of the capacitor to the component's ground pin. This topology assumes a single- or double-sided layout is provided, typical of board without power and ground planes. For a dual inline package (DIP), a very long trace perimeter will always exist due to physical constraints, regardless of the actual location of the capacitor —either near the power or ground pin, the loop perimeter remains the same.

It is extremely difficult, if not impossible, to optimally calculate the value of charge a capacitor is to provide to minimize power or ground bounce due to lack of parametric data. This is in addition to not knowing how much switching noise is injected into the power distribution system when the total amount of current required is not specified in data sheets for use under maximum capacitive load conditions (always an unknown value). To accommodate for unknown parametrics, selection of a 0.1 µF capacitor is commonly made. This selection is generally based on historical reasons, not functionality concerns or the mathematics related to engineering analysis and design.

DEVELOPMENT OF RF COMMON-MODE ENERGY

Common-mode energy is developed as a result of a differential-mode imbalance within a power and ground distribution network. A propagation path includes interconnects and other components. Undesired energy can be either a voltage- or current-driven source into an antenna structure. Power and ground planes can be visualized as a dipole antenna, with the power rail at voltage potential (one-half of the dipole) and the 0V-reference at ground potential (the other half of the dipole). When an imbalance between power and ground exists, residual RF energy will drive the antenna, allowing undesired common-mode RF to propagate as electromagnetic interference (EMI).

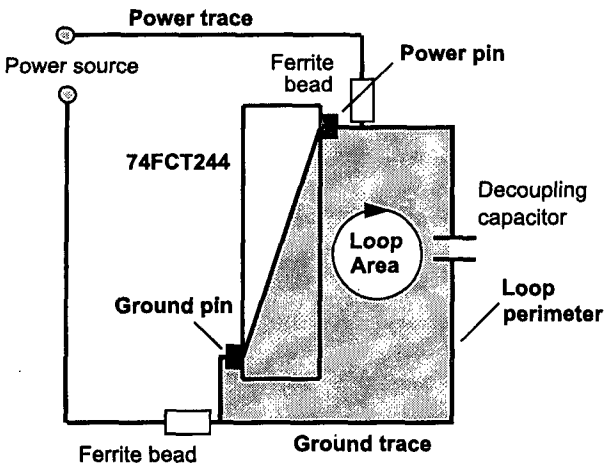

Figure 1. Loop perimeter from capacitor placement.

Another way to visualize power and ground planes as transmission lines within a PCB is to take these very wide planes and physically shrink them down to the width of a trace. Conversely, take a standard trace and make it infinitely wide. One can see that power and ground planes must be treated as transmission lines, the same as a pair of traces with a source and return path.

If power and ground is in perfect balance (differential-mode), common-mode energy cannot exist, which rarely occurs in an actual product design. An example of this configuration is shown in Figure 2. Inductance in either the voltage or ground network allows a voltage potential difference to occur between two points. This voltage potential difference causes common-mode energy to be developed as a result of the inductance in the transmission path. The inductance in Figure 2 is the trace routed between component and decoupling capacitor.

In the figure, the item identified as "interconnect" refers to anything connected to the circuit, which includes I/O connectors, another component, or a decoupling capacitor. All interconnects provide a capacitive load. The RF noise source (74FCT244) is connected to a battery. The decoupling capacitor shares the same power and ground structure, isolated from the battery by ferrite beads. The key item to visualize is the configuration and topology of the circuit shown, along with a simplified concept presented. The interconnect shown in the figure is physically located at the end of the trace route, regardless of trace length.

WHY THE DECOUPLING LOOP RADIATES

The physical configuration of both the component and the decoupling capacitor with an interconnect trace between the two is illustrated in

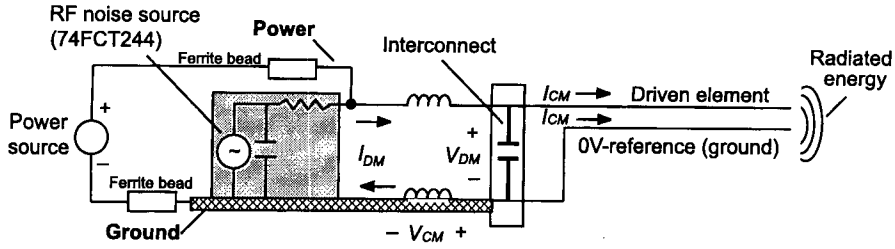

Figure 2. Development of common-mode energy from differential-mode imbalance.

Figure 3.

The power trace acts as the driven element that allows common-mode RF energy, as a result of inductance within the network, to drive a dipole antenna. In addition, the inrush surge of current when the component switches logic states causes an additional strain in the power and ground network, thus exacerbating development of common-mode energy. This occurs only when insufficient decoupling or use of an incorrectly chosen discrete capacitor is provided.

Any trace from the lead bond pad of a component to the decoupling capacitor will energize the dipole antenna. This occurs even if power and ground planes exist, as long as there is a routed trace between the capacitor and component. If the mounting pads of both the component and capacitor (interconnect) are via "directly" to the power and ground network without a routed trace between the two, this discussion and analysis become moot!

TIME DOMAIN ANALYSIS

Research[2–4] shows that a lumped model can be used to describe a power and ground plane structure. This lumped model is valid only when analyzing multilayer stackup assemblies and assumes that a sufficient number of decoupling capacitors is provided to give exactly the correct amount of charge to a theoretical model. This type of simulation rarely represents an actual PCB design and layout (theoretical versus real life).

There are several aspects that one must consider when selecting a decoupling capacitor; the self-resonant frequency and amount of charge available to digital components. We first examine self-resonant frequency.

SELF-RESONANT FREQUENCY

Equation 1 defines the theoretical value for the self-resonant frequency of a capacitor. Selection of a capacitor based entirely on this equation means incorrectly choosing a component for a specific pulsed excitation frequency that may not provide optimal benefit.

$$\omega = \frac{1}{\sqrt{LC}} \qquad f = \frac{1}{2\pi\sqrt{LC}}$$

$$C = \frac{\left(\frac{1}{2\pi f}\right)^2}{L} \qquad (1)$$

where

C = capacitance (Farads)
L = inductance (Henries)
f = frequency (MHz)
ω = 2πf

Selection of a 3.9 nF capacitor for use in this experiment proved to be an interesting choice. The desired operating frequency was 80 MHz, placed into Equation 1 with 1 nH lead inductance. By using a non-typical capacitor value, radiated RF emissions from the decoupling capacitor layout, and the dipole effect would never have been discovered.

A portion of this analysis is based on the self-resonant frequency of a capacitor. Figure 4 illustrates two different plots using Equation 1 in its pure form—no equivalent series resistance (ESR) included.

The switching speed of a component does not change; however, the effectiveness from use of a particular decoupling value is diminished when the minimal value of impedance does not match the spectral distribution range of the switching device. The key design requirement is to ensure that very low impedance exists between power and ground within the frequency range of interest. Outside this spectral range, the impedance value becomes too large to be of benefit, thus functionality and EMI is compromised. The magnitude of impedance must be low enough for optimal transfer of voltage and current.

CHARGE DISPLACEMENT

The physical placement of a discrete decoupling capacitor with respect to components within a reasonable distance is, in reality, not critical. This condition is valid "only" if both power and ground planes are

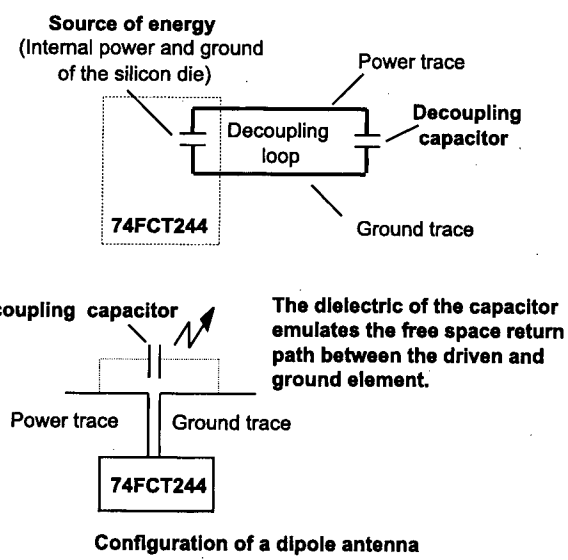

Figure 3. Decoupling loop radiating as a dipole antenna.

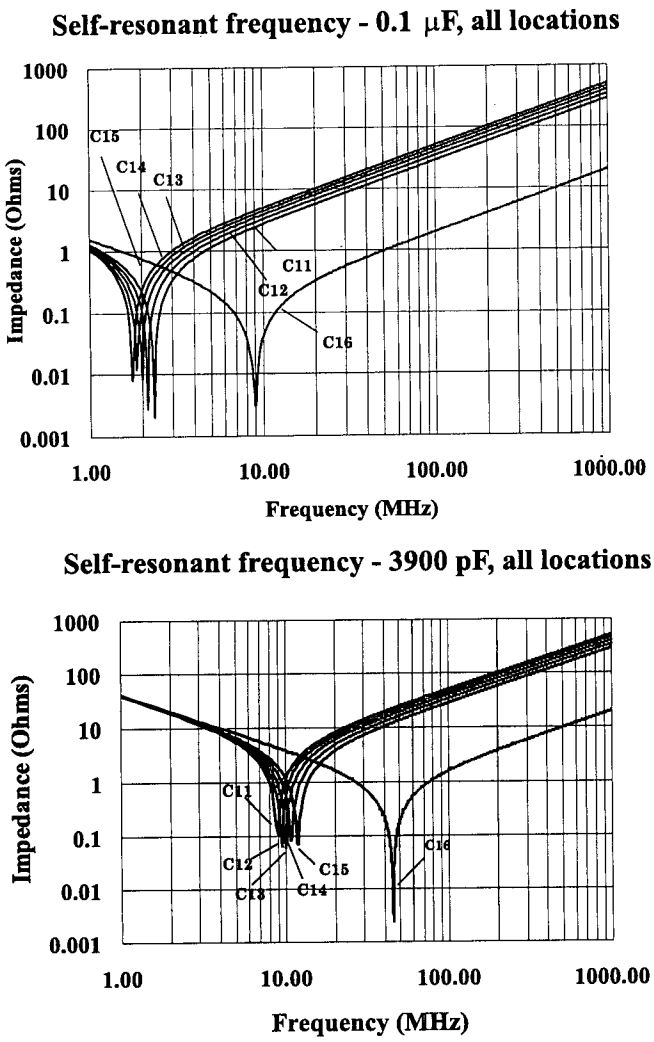

Figure 4. Capacitor self-resonant frequency plots.

provided; and if no routed trace exists between capacitor and the component, only vias built directly into the mounting pad from the device to the planes. Since energy charge from a capacitor propagates in a radial fashion within a planar structure, all components within the vicinity of the capacitor will receive the same amount of electrical charge at approximately the same time.

A transient surge of current within planes spreads radially from its source stimulus. The magnitude of this electric charge decays with distance. This is true only in the transient sense. For repetitive or periodic excitation within a transmission line (power and ground planes), due to the finite size of the assembly, a loss of charge energy occurs. This energy loss exists due to the dielectric properties of the assembly. A lossy structure will suppress resonances created by various capacitive networks (discrete capacitors, parallel capacitors, and the power and ground plane pair). The steady-state transfer impedance presented to the distribution network must be sufficiently low throughout the entire frequency spectrum. Anti-resonant peaks are generally larger than the magnitude of impedance at the point of excitation. At a remote location from an excitation point, RF energy may actually be greater than the stimulus itself.

Energy to components travels at a propagational speed that is exclusively dependent on the dielectric value surrounding the planar material. For the microstrip topology, propagation delay, t_{pd}, is 1.67 ns/ft (0.24 ns/cm). This value is based on a dielectric constant (ε_r) of 4.3, calculated by

$$t_{pd} = 1.017\sqrt{0.475\varepsilon r + 0.67} \qquad (2)$$

With a physical loop dimension of 4.5 inches (11.4 cm), it takes only 0.63 ns for charge energy to travel from capacitor to component. Assuming a 1 ns switching rate, charge energy reaches the component in approximately 63% of the time period available before the next edge transition, even at this extremely large distance separation (4.5 inches or 11.4 cm). Therefore, the exact location of the capacitor relative to a specific component is not critical, as charge energy will be available for all but the worst layout topologies. This is again valid "only" if planes are provided—there is no routed trace between capacitor and component (vias built into the mounting pads).

If a capacitor is located physically closer, the component will receive charge energy in even less time, which is highly desirable. When a decoupling capacitor is located physically adjacent to the source driver, it takes only sub-picoseconds for charge energy transference to occur. This is the primary reason why decoupling capacitors can be located anywhere in the vicinity of switching devices. Digital components and deoupling capacitors must be connected directly to the power and ground planes—no routed traces between devices for this layout technique suggestion to work.

Although this layout suggests that placement of a decoupling capacitor can be anywhere within the vicinity of the component, this condition is not possible for real product designs (not manufacturable).

The inductance in a routed trace between the decoupling capacitor and component allows for a voltage-potential gradient to be established between the two. This voltage-potential gradient is one reason how common-mode RF energy is developed within a PCB. Other causes of undesired common-mode energy within a PCB include switching activity directly from the silicon die propagating through the component's plastic package, trace routing topology, purity of the supply voltage, physical characteristics of the board material, and dielectric properties of the decoupling capacitor.

ENERGY CHARGE STORAGE

A power distribution system must be capable of

providing sufficient charge to all components at the same time. There is a finite period when the power distribution network is unable to operate efficiently. This finite period is due to the effects of logic crossover between transition states internal to the silicon wafer.

Logic crossover refers to the process of internal gates transitioning from high-to-low (or vice versa). During this period, when the edge transition is exactly between high and low, a direct short between power and ground occurs. Detrimental effects on the PCB during this condition are exacerbated when many components must source drive current to multiple output loads at the same time. If power and ground are provided using routed traces, typical configuration of single- and double-assemblies, functionality concerns develop. These concerns are minimized by use of solid power and ground planes containing low-inductance through-hole vias to both component and capacitor.

The impedance of solid planes is magnitudes less than a routed trace (picoHenries for planes versus nanoHenries for traces). The problem is that not every design or layout will have solid planes available, and in many cases, routed traces must be utilized due to package configurations (lead bond versus non-lead bond). This occurs regardless of stackup assignment: single-sided, double-sided or multilayer.

Many device packages require a routed trace for connection from the lead-bond pad to the power and ground planes. For BGA and flip chip applications, the need for routed traces does not exist. The concern herein lies with devices that have lead-bond wires.

Planes are "assumed" by many engineers to be capable of providing unlimited energy charge to all devices within a layout. This unlimited capability should minimize use of discrete components. Simulation of complex structures cannot accurately calculate actual storage capacity required. Inrush surge current is needed only during a state transition.

Equation 3 defines the amount of stored energy required for minimizing board-induced switching disruption. The correct amount of capacitance required to minimize RF switching noise injected into the power and ground distribution network is given by Equation 4.

Determining actual values for the variables in Equations 3 and 4 is nearly impossible due to unpublished vendor data. The complexity of solving these equations increases when multiple devices operating on different voltage rails are used.

Because solving Equations 3 and 4 is nearly impossible, engineers commonly use 0.1 µF capacitors for decoupling. This is based mainly on historical reasons and not on the mathematics of engineering. Although this value may be totally incorrect, or be magnitudes greater or less than necessary, they are still useful when viewed on a system-wide basis.

$$Q = CV_c \text{ (Coulombs)} \qquad (3)$$

$$C = \frac{I_c\, dt}{dV_c} \quad (Farads)$$

$$(or)$$

$$I_c = C\frac{dV_c}{dt} \quad (Amps) \qquad (4)$$

where

Q = total charge
C = capacitance
V_c = voltage of circuit (volts)
I_c = capacitor current
dt = change in unit time
dV = change in voltage per unit time, dt

For most applications, use of 0.1 µF capacitors affects the performance of the power and ground system in a distributed manner for the entire assembly, and not just for discrete devices that are located adjacent to the capacitor. The reason why these capacitors appear to work efficiently is due to the radial distribution of charge energy rippling throughout the overall assembly, which is an event not recognized throughout the engineering community.

Parallel Decoupling

When using capacitors in parallel, the total capacitance (stored charge) increases in direct proportion to the number of components provided. At the same time, the equivalent series inductance (ESL) and equivalent series resistance (ESR) decreases inversely.

Lower values of ESL and ESR enhances overall performance of decoupling capacitor networks by ensuring that sufficient charge current is provided by the power and ground distribution system in a more efficient manner. This efficiency occurs because of a lower magnitude of impedance at a particular switching frequency mandatory for functionality of digital components.

As the amount of stored energy increases, board-induced power and/or ground bounce is minimized. This bounce minimization enhances signal integrity while also minimizing development of RF radiated energy.

For the test PCB investigated herein, Table 1 illustrates the effects of insufficient decoupling related to power and ground bounce. For all configurations, bounce was excessive, causing the device to not function properly. This means that signal integrity of a data transition is not assured.

An unbalanced power and ground network means that the differential balance of the power distribution system is impacted. Regardless of the inefficiency of the loop area as an antenna, radiated EMI still exists.

Board-level induced switching noise (caused by bouncing either power or ground internal to the device package, but observed on

Configuration	Bounce Level	RF Emissions
No decoupling	1.6 V	minor[1]
C11 (3900 pF)	506 mV	maximum
C12 (3900 pF)	588 mV	maximum
C13 (3900 pF)	590 mV	maximum
C14 (3900 pF)	634 mV	maximum
C15 (3900 pF)	670 mV	maximum
5-1000 pF (0.005 µF total)	164 mV	minimum
5-3900 pF (0.02 µF total)	467 mV	moderate
5-0.1 mF (0.5 µF total)	506 mV	moderate

[1]The reason for minimal emissions is because once the voltage level drop exceeded 250 mV (4.75 V with a 5 V bench voltage), the device stopped working. Most bounce levels exceeded functional parameters, thus the device stopped working during an edge transition event. Signal integrity was not investigated nor assured.

Table 1. Functionality effects due to power/ground bounce.

the PCB), is one reason for the development of common-mode RF energy.

It is interesting to note that, regardless of physical placement of the decoupling capacitor(s), from best to worst location, C11-C15 (2.5 inches to 4.5 inches), radiated RF amplitudes were identical (refer to Part 1 of this article for details). This identical value occurred because the same magnitude of energy charge was provided by the single capacitor regardless of physical location. The energy charge, traveling from capacitor to component, was well within the time period between logic state transitions.

When additional charge energy was provided by five capacitors simultaneously, all with the same value, a significant reduction in radiated RF energy was observed. This validates the need to provide sufficient charge to maintain the power and ground planes from bouncing. It becomes imperative at this time to calculate the proper value of capacitance required. This is not easily achieved when using Equations 3 and 4.

When no decoupling was provided (Table 1), radiated emissions were not significant. This is because the device was never fully powered on. The reason for power off was due to a 50% duty cycle input, causing a significant bounce condition to occur along with an excessive voltage drop, related to the bench voltage.

Power Consumption

The 74FCT244 consumed considerable input current when fully loaded and when all drivers switched synchronously in addition to quiescent current through a fixed impedance network (power and ground). The input voltage dropped well below that required for functional operation. When a decoupling capacitor was provided, additional current draw occurred from the power supply, which exacerbated this situation. However, the charge storage capacity from the capacitor helped keep the 74FCT244 from seriously affecting the power/ground network by minimizing board-induced noise and ground bounce.

At the same time, radiated RF energy from switching events caused common-mode RF energy to develop due to routed trace inductance between capacitor and component. RF energy now has the opportunity to propagate from the PCB using the dielectric of the capacitor as the transmission media between the driven element and ground reference of the dipole antenna structure.

In order to ensure functionality, the +5 VDC bench supply cannot drop more than 250 mV during an edge transition. Supply voltage margin requirements differ between logic families. The measured voltage drop significantly exceeded 250 mV.

Vendor data sheets do not specify the total charge required to minimize power or ground bounce when devices are operated under a maximum capacitive load.

When a sufficient amount of electrical charge is available from capacitive structures during a state transition, by discrete components or planes, and the self-resonant (switching) frequency of the capacitive network is approximately equal to the operating frequency of the component, optimal decoupling performance may be achieved. This occurs only if the magnitude of impedance of the network is below a required target level for all frequencies of concern.

A 74FCT244 under maximum load mandates approximately 0.02 µF of capacitance for optimal performance. However, use of 0.1 µF is commonly found in product designs, as many engineers do not understand the need for calculating an optimal value required for decoupling. Usually, there is always too much capacitance provided, which may not be bad under certain conditions.

If power and ground planes are implemented, along with discrete capacitors, both must have enough storage capacity for all logic state transitions before the capacitive network receives a recharge from the external power supply.

During the period that the power and ground network becomes unstable due to lack of energy

storage, or when the decoupling capacitor is at a minimal voltage level, common-mode RF energy will be developed. This is the primary reason why decoupling is critical for operational performance in any digital system.

It takes a power supply a long time to recharge a capacitive network. This network consists of both decoupling capacitors and the power and ground planes. Both capacitive structures must be able to store sufficient electrical charge to sustain multiple transitions (millions of edge transitions) before the power supply can recharge the planes. If any edge transition occurs when the capacitive network is low on electrons, common-mode RF energy will be injected into the routed trace between the decoupling capacitor and the component.

A typical power and ground distribution system must provide significant electrical charge within a very small time period. The velocity of propagation of energy between capacitor and driver is extremely fast, especially if located within 4.5 in. (11.4 cm). This is why lumped analysis is possible for simulation purposes. Capacitance is distributed throughout an assembly, which benefits multiple components at the same time within the radius charge circle of the localized storage capacitor.

Digital devices switch logic states synchronously, which places a significant strain on the supply distribution network. A remote power supply cannot respond fast enough to replenish this distribution network due to a typical high impedance in the interconnect between power supply and PCB. In addition, the power supply generally contains electrolytic capacitors to minimize ripple and power dropout. These capacitors cannot replenish electrical charge at switching frequencies. EMI will always be present, no matter what decoupling methodology or topology is implemented.

RECOMMENDED LAYOUT STRATEGIES

Figure 5 provides layout recommendations when using discrete capacitors for the purpose of decoupling.[5] The key item to note is that there should be minimal or no inductance between capacitor and component, especially from a routed trace. A via has a typical inductance value of 1–3 nH. This inductance is significantly less than a very short length of routed trace "and" its respective via.

It is recommended that multiple vias be used at the same time, or that a single via have as large as physically manufacturable dimensions to ensure that the lowest inductance value is present at all times (Figure 6).

SUMMARY

Development of common-mode radiated energy within a PCB occurs due to complex parasitics and layout topology. Many of these parasitics are generally unknown to design engineers. A voltage drop across inductance in a transmission line develops common-mode energy. This transmission line is identified as either voltage and/or ground. Decoupling capacitors, used to minimize development of RF energy, and to ensure signal integrity may be one source of allowing common-mode EMI to be developed and propagated.

The physical dimensions of a decoupling loop, due to capacitor placement, does not play a role in the magnitude of RF emissions propagated from the decoupling circuit when applied to a typical PCB layout.

Traces by themselves cannot radiate unless a dielectric media exists to transfer an electromagnetic field from a driven source to a

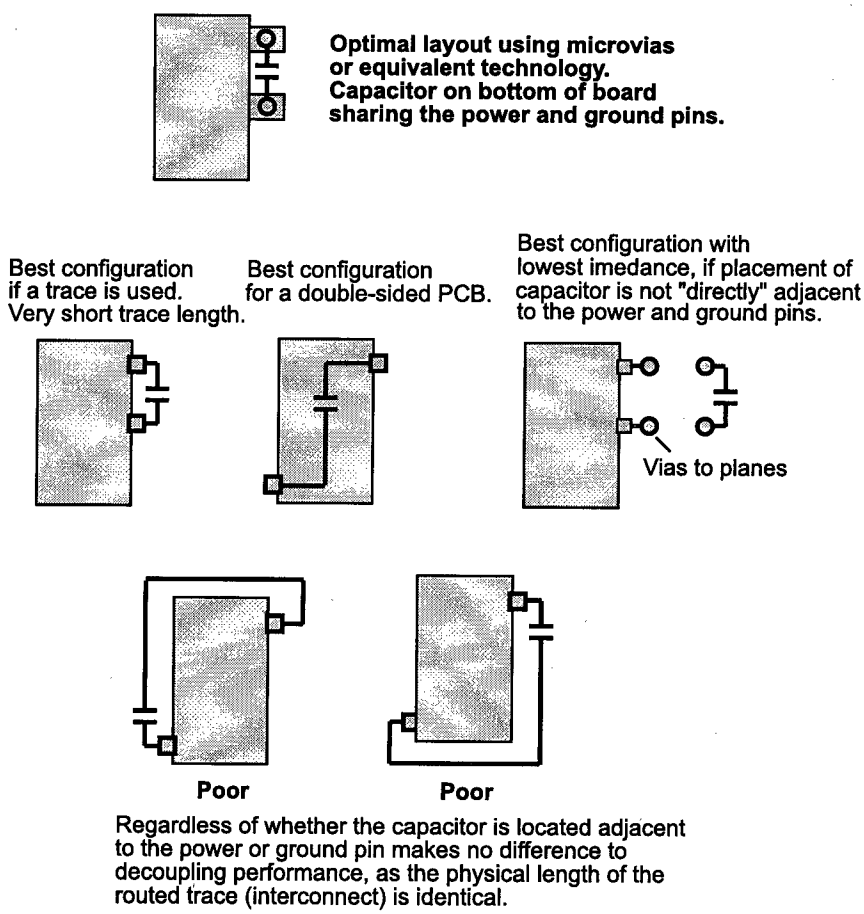

Figure 5. Capacitor placement recommendation.

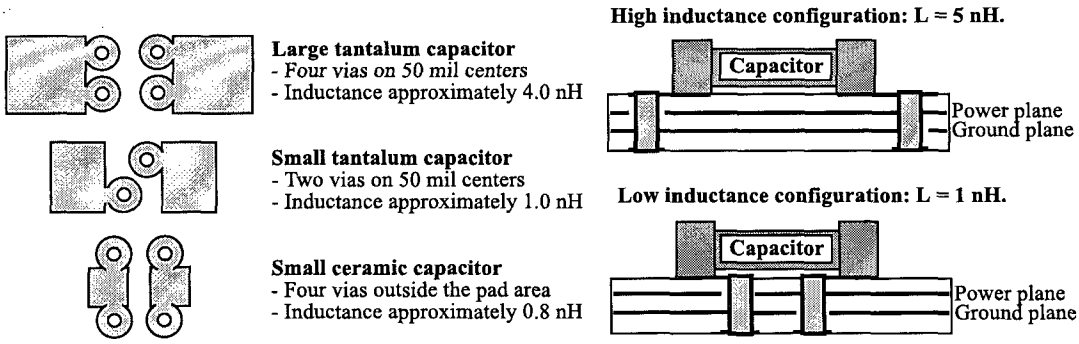

Figure 6. Capacitor placement patterns for optimal performance—multilayer implementation.

return. The decoupling capacitor closes the RF loop, allowing an electromagnetic field to propagate as EMI. The dielectric material of the capacitor emulates free space, permitting a dipole antenna structure to radiate common-mode RF energy as a result of decoupling implementation. Common-mode energy within an unbalanced differential power and ground distribution network now propagates into free space.

The size of a decoupling loop determines the frequency of propagational efficiency. The physical dimensions of decoupling loops for most PCBs is an inefficient antenna below 2 GHz, yet low frequency EMI is observed.

Once a capacitor is applied to a PCB, the self-resonant frequency will decrease significantly, thus minimizing its effectiveness as a decoupling element due to excessive trace inductance. The magnitude of impedance also changes, making the capacitor less effective at the frequency range of interest.

If power and ground planes are provided, development of common-mode RF energy will be minimized due to efficiency in providing a localized charge of energy. This localized charge is distributed throughout the assembly. The low impedance of planes means that there will be a very small voltage drop between components and their power source. Differential-mode balance is ensured, as long as all digital components do not consume more energy than both the planes and decoupling capacitors are capable of providing.

Classic methods for selection of a decoupling capacitor are now partially ineffective for optimal prevention of noise in power and ground networks, in addition to reducing radiated emissions and minimizing board level noise voltage. One must calculate, not randomly choose the correct value of a decoupling capacitor.

Use of parallel capacitors will increase charge energy proportionally to the number of capacitors. Lead inductance is reduced inversely.

Close physical spacing of power and ground planes allows for a very low impedance transmission line to be present with a high value of capacitance.

The magnitude of disturbance caused by a sudden demand for current, due to components switching logic states, reduces rapidly as the distance from the demand point increases. This area increases as the square of the radius increases.

SOLUTION TO REDUCTION OF RADIATED EMI

The key item of concern is to not allow common-mode RF energy within the power and ground distribution network to develop. If routed traces are provided between the capacitor and the component, common-mode energy within this distribution network will radiate from a dipole antenna structure due to the use of routed traces. The decoupling capacitor allows RF energy to propagate from the driven element to ground.

Three aspects must be considered when selecting a decoupling capacitor. First is series resonance. A minimum value over a large spectral bandwidth provides a low impedance path for power and ground distribution, ensuring functional operation of digital circuits.

The second aspect deals with the need to provide sufficient energy charge to switching components in an effort to minimize development of common-mode energy.

The third aspect is the interaction between capacitors in parallel. At a particular frequency, the anti-resonant impedance of parallel pairs becomes very high (parallel resonance). This is because one capacitor has become inductive and the other is still capacitive.[5, 6] At a particular frequency, these two capacitors converge, causing a high value of impedance to exist. The magnitude of this anti-resonant frequency is a direct function of ESR. The lower the ESR, the higher the magnitude of this anti-resonance response in addition to a lower magnitude of impedance at the zero or self–resonant point.

If using multiple low ESL/ESR parts for decoupling, ensure that the ESL/ESR is as low a value as possible. Include device package parasitics. Mounting inductance is primarily dependent on device configuration, as well as via length and power plane spacing. Inductance is a function of the loop area of the current path, as well as the spreading inductance internal to the planar structure. The inductance contributed by the internal intercon-

nects within the capacitor package is a very small part of the total network impedance.

By properly designing various components of the power distribution system (power supply, bulk capacitors, decoupling capacitors, and plane stackup), using a knowledge of operational parameters, one can implement a power distribution system that exhibits very low impedance from 10s of Hertz, up to 100s of MHz. It is possible to design a decoupling methodology that operates up to the GHz range.

Recommended procedures to select a decoupling methodology to reduce radiated emissions, minimize board level noise, and enhance signal integrity are detailed below. When designing a power distribution network, the goal is to maintain very low impedance across a large spectral bandwidth while providing sufficient energy charge. Typically, the capacitive value selected for decoupling is determined well before layout is finalized or mathematical analysis considered. Selection is generally based on historical usage, not on how the device is to function within its intended application.

Incorrect selection of discrete decoupling capacitance will allow RF energy to radiate from routed traces between capacitor and component.

1. Connect all decoupling capacitors directly to the power and ground planes by through-hole vias. Vias are preferred over routed traces due to significantly less inductance in the decoupling loop.
2. Selection of a decoupling capacitor must first be made by determining the maximum amount of energy charge required for minimizing voltage fluctuations, and to maintain pure differential balance between power and ground. This is the most difficult behavioral model to acquire or determine. Use Equations 3 and 4, based on actual or unpublished parameters.
3. Calculate or measure actual loop inductance, including bond wire and lead frame connection (internal to the component package).
4. Physical measurement of actual loop inductance may not be practical for many layout configurations. Calculate the self-resonant frequency of the decoupling capacitor using Equation 1. It is not the actual specific frequency that is important, but the spectral frequency range of operation of the capacitor before the capacitor starts to behave inductively.
5. The magnitude of impedance presented to the power distribution network is the primary item of concern. The magnitude of impedance must be very low over a range of frequencies both above and below the self-resonant frequency point.
6. For parallel decoupling, select values that will resonate over a large frequency spectrum while maintaining low impedance throughout the frequency spectrum. Use of parallel decoupling of the same value allows for a greater amount of charge energy to be present. The magnitude of impedance will also be significantly reduced.
7. In order to implement a decoupling methodology, using proper engineering analysis, one must bounce back and forth between time domain and frequency domain calculations until both domains converge to an optimal value for enhanced signal integrity while minimizing radiated EMI.

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