IC Design Techniques to Achieve EMC in Electrical Systems

ANJAN SEN AND ANDRE WALKER
Zilog, Inc., Campbell, CA

INTRODUCTION

Until recently, suppression of electrical noise has primarily been the concern of systems engineers. However, as device operating/switching speeds increase well into the megahertz range, electromagnetic compatibility (EMC) has become a growing concern for IC manufacturers and vendors. Shielding, strategic layout of printed circuit boards (PCBs), and use of noise filters are often employed at the system level to suppress noise. This article discusses several complementary metal oxide semiconductor techniques used to minimize conducted and radiated emissions at the IC level.

NOISE IN ICs

For a system containing a microprocessor or microcontroller, peripheral devices, and high speed logic, the EMI level can be anywhere from acceptable to extremely high. Certain applications can tolerate high levels of EMI while others, such as consumer and automotive applications, cannot. In EMI sensitive systems, the need for noise filters and shielding can be reduced if EMI inherent to the ICs is minimized.

The most common forms of noise, conducted or radiated, in a high speed digital circuit are the voltage spikes on the power and ground lines. Any static outputs which are at V_{dd} or ground will also exhibit these spikes. This noise usually occurs at harmonics of the clock frequency (Figure 1). In a microcontroller, for example, every edge of the clock causes thousands of internal transistors to switch states. In addition, output transistors, which source and sink high current, may also switch. This large rate of change of current, or d_I/d_t, results in spikes in the V_{dd} and ground bus.

In EMI sensitive systems, the need for noise filters and shielding can be reduced if EMI inherent to the ICs is minimized.

Figure 2 shows a CMOS output driving a capacitive load and Figure 3 shows a simplified equivalent circuit which takes the package lead inductance into account. L_p is the inductance of the power lead(s), L_g is the inductance of the ground lead(s), and L_o is the inductance of the output lead. Typically, L_p, L_g, and L_o are 3 to 20 nH.

Figure 4 assumes that C_{load} is fully charged, the p-channel

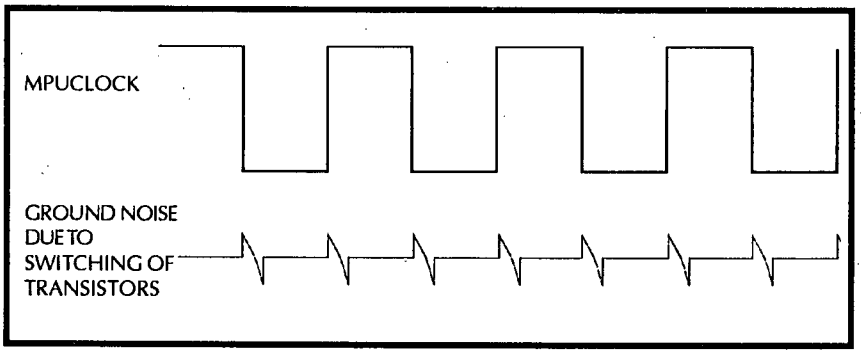

FIGURE 1. *Switching Noise on Power and Ground Lines.*

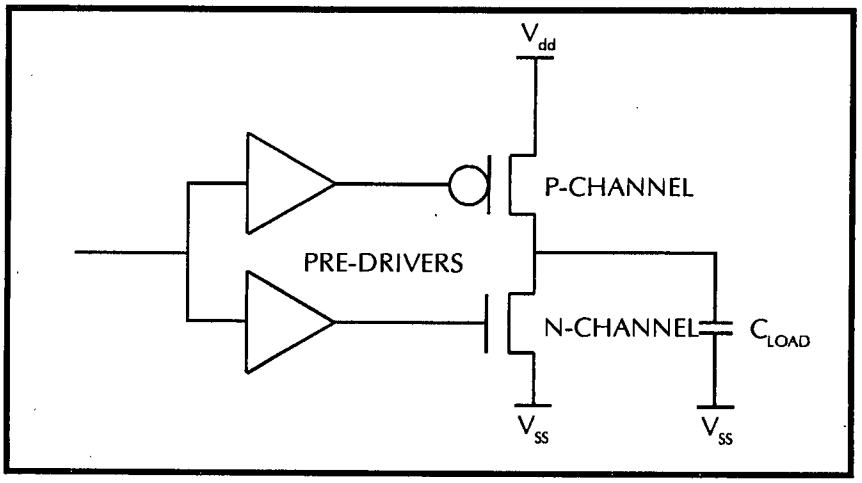

FIGURE 2. *CMOS Output Driving a Capacitive Load.*

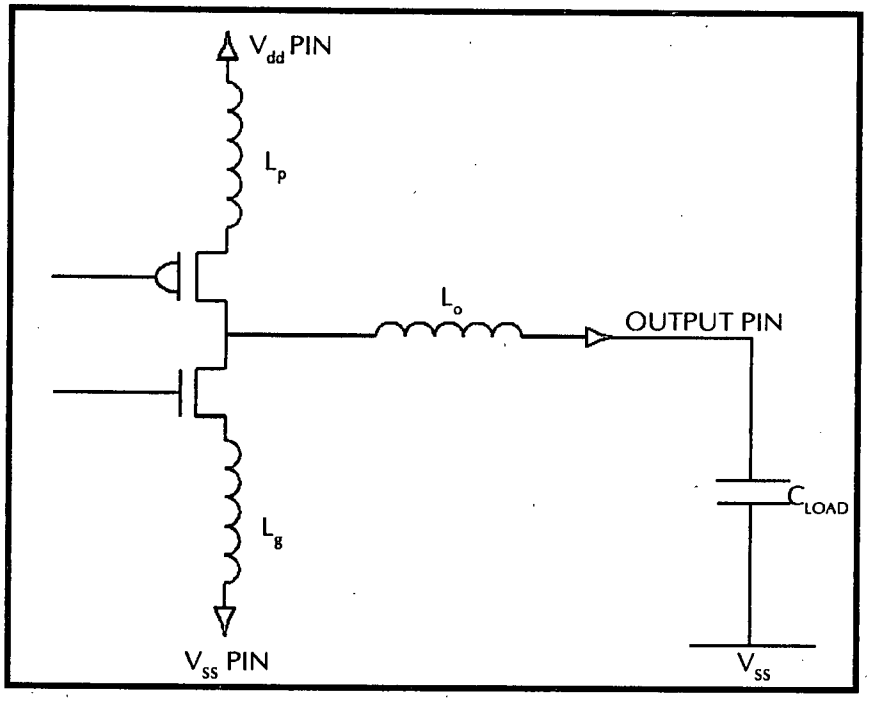

FIGURE 3. CMOS Output Including the Lead Inductances.

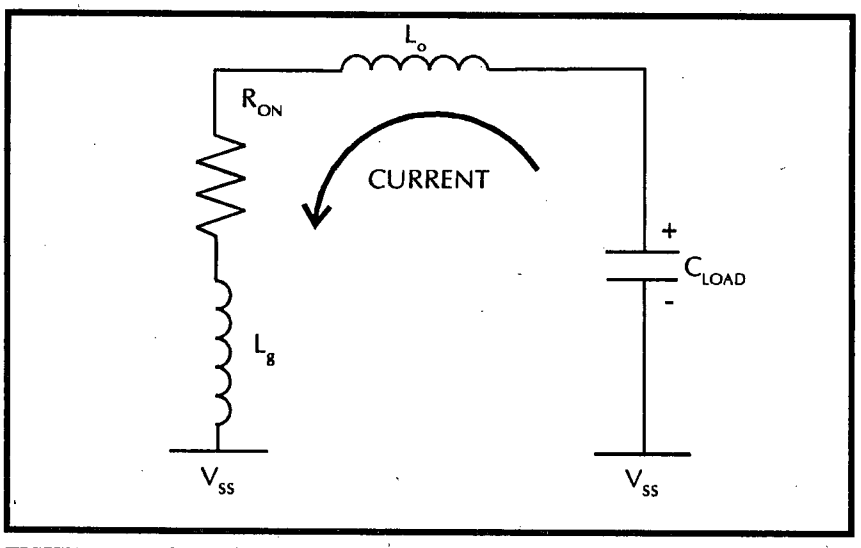

FIGURE 4. N-Channel is On: P-Channel is Off.

transistor has just switched off, and the n-channel transistor is beginning to turn on. As C_{load} begins discharging, the current through L_g starts to change. This d_i/d_t induces a voltage across L_g (Equation 1) which causes the chip's internal ground reference to deviate from the board's ground reference. Any of the device's static outputs which are in the low state will also show this ground bounce. This may subsequently cause false triggering to other devices. In addition, the ground bounce may result in the malfunction of the device itself since all inputs to the device are referenced to the chip's ground which is now varying. Noise on the V_{dd} bus occurs due to similar reasons.

$$V = -L\, d_i/d_t \qquad (1)$$

The amount of ground bounce, and hence the strength of the radiated/conducted emissions, increases as the number of simultaneously switching outputs (such as address and data lines) increase.

In the case of radiated noise from a signal such as an address or data line, the bandwidth of the radiated EMI depends on the transition time of the signal. The bandwidth reduces as the transition time increases. This means that fast switching output drivers can result in radiated EMI that covers a large span of the frequency spectrum. The energy level of the noise spectrum increases as the voltage swing increases. For example, one output of a microcontroller switching between 0 and 5 V would produce EMI with field strength less than an open drain output of the same microcontroller switching between 0 and 15 V. If traces on the PCB or the leads of the IC package are the appropriate length, they can function as efficient antennas, thereby increasing the field strength of the radiated EMI.

Suppression of radiated noise is particularly important in applications which involve transmission/reception of data by radio waves. Examples are television, radio, and cellular telephones. In some cases, the application may pass the FCC emission tests but radiated emissions may still be high enough to cause application specific problems such as sensitivity loss in cellular telephones.

The two sources of noise for a high-speed device (a microcontroller for example), that have been considered so far are:

1. Switching noise on the power and ground lines due to a large rate of change of current (d_i/d_t). This noise is conducted and radiated.

2. Outputs with fast edges radiated by a conductor acting as an antenna.

NOISE REDUCTION METHODS

Noise levels can be minimized by reducing any inductances that output signals encounter, and by reducing the rate of change of current (d_i/d_t) in a device.

REDUCING INDUCTANCES

To minimize voltage spikes on the V_{dd} and ground lines, several precautions can be taken. Equation (1) demonstrates that if the V_{dd} and ground lead inductances are reduced, the voltage spikes will be reduced proportionately. Figure 5 shows a 24-pin lead frame and the inductance associated with each pin. The shorter the lead length, the less the inductance. Therefore, it is preferable to use the pins with the shorter leads for V_{dd}, ground, and high speed outputs. To further reduce the V_{dd} and ground inductances, additional V_{dd} and ground pins could be introduced.

For ICs such as bus drivers and octal latches, where outputs of one device feed the inputs of the next device in a daisy chain configuration, all inputs should be on one side of the device and the outputs on the other (Figure 6). This minimizes PCB trace lengths, thereby reducing inductance.

REDUCING THE CURRENT RATE OF CHANGE (D_i/D_t)

Another method of reducing noise on the V_{dd} and ground lines is to limit d_i/d_t. This can be done by either reducing I (that is, the current sunk or sourced by an output) and/or increasing the time taken to reach the peak value of I. This can be achieved by the following techniques:

Reducing the Size of Output Transistors. The current, I, may be reduced by increasing the on-resistance of the output transistors. Figure 4 illustrates that the RC time constant would

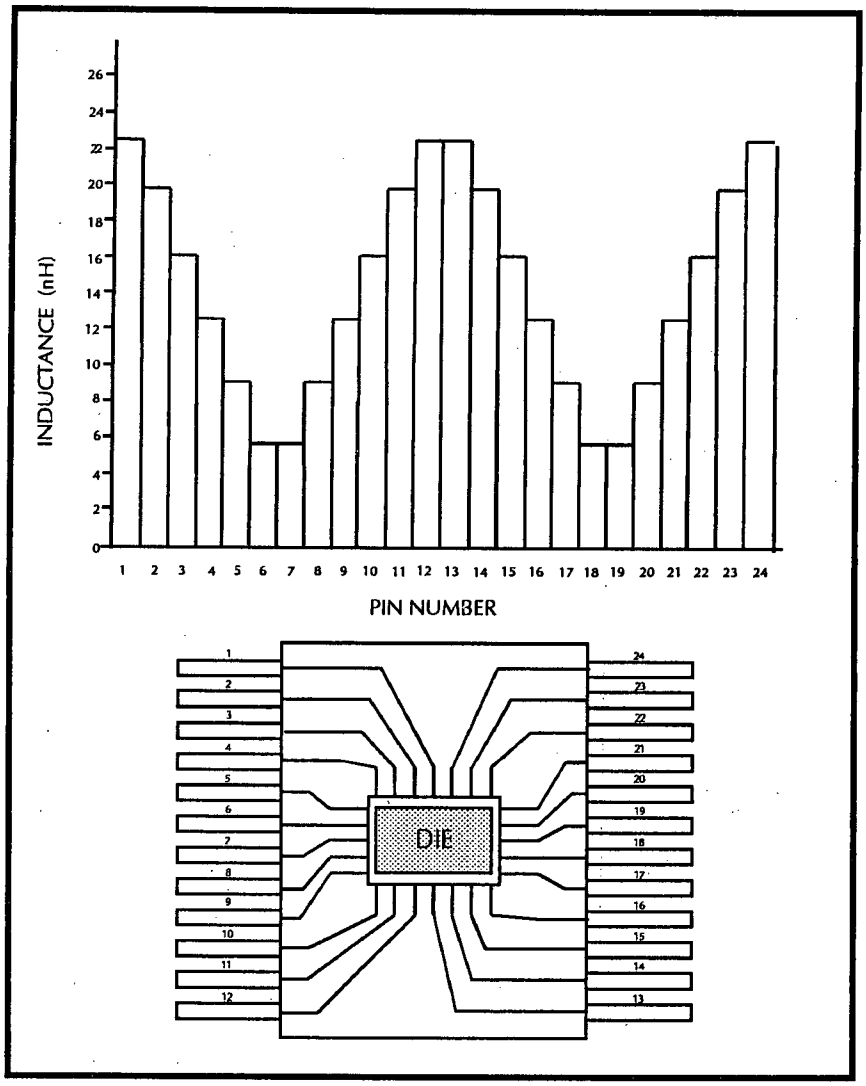

FIGURE 5. *Lead Frame Inductance for a 24 PIN DIP.*

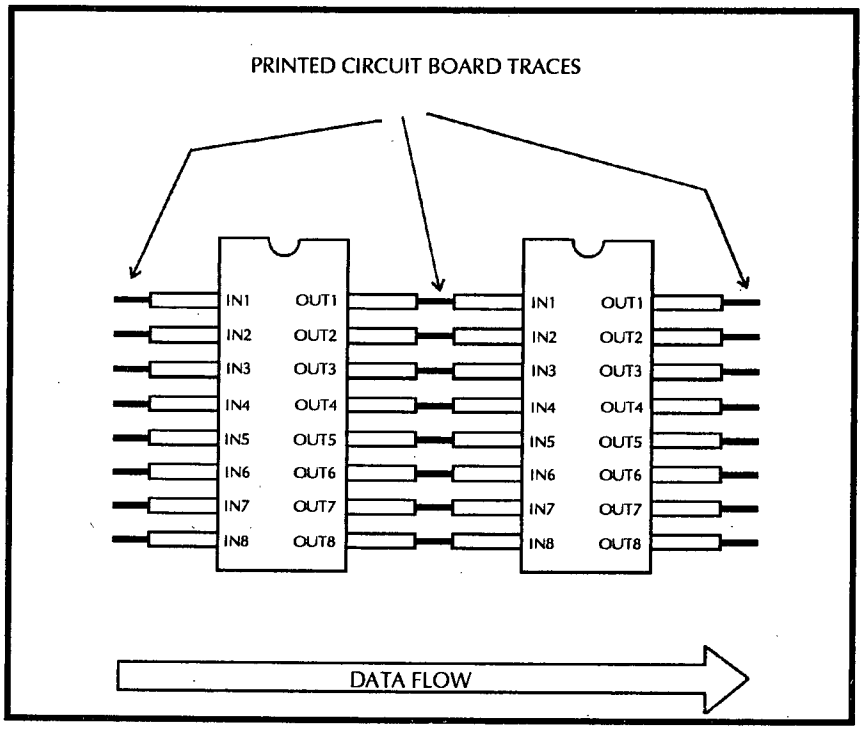

FIGURE 6. *Pinout Allows Minimum PCB Trace Lengths.*

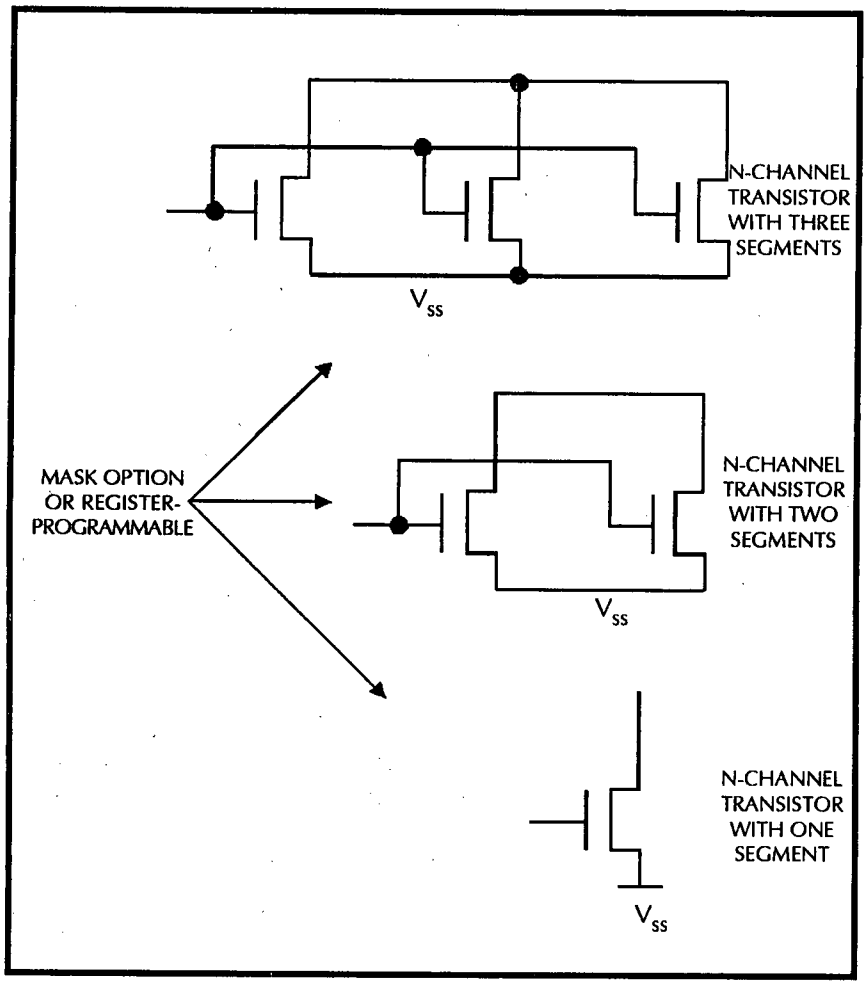

FIGURE 7. *Programmable Output Transistor (N-Channel Shown).*

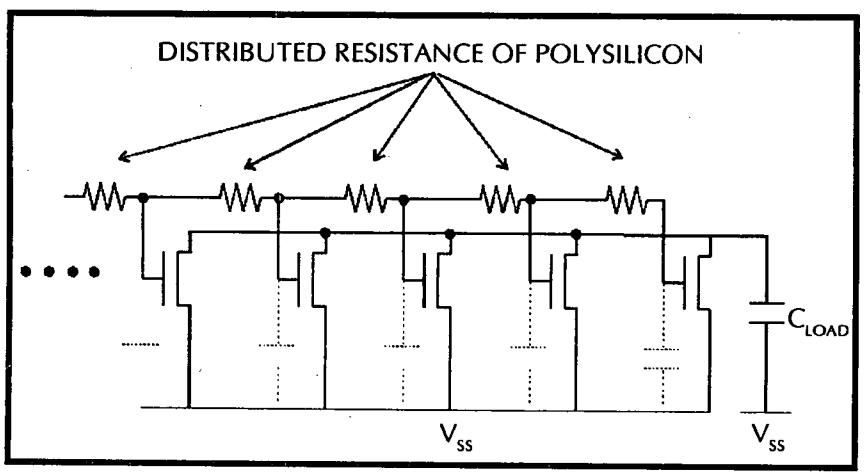

FIGURE 8. *N-Channel of Distributed Transistor.*

increase and C_{load} would charge and discharge at a slower rate. The slew rates of output transistors would also be reduced, as shown by Equation (2). This means that the bandwidth of radiated emissions would be reduced.

$$I = C\, d_v/d_t \qquad (2)$$

This solution may not work in all cases since the current handling capability of output transistors is somewhat sacrificed. Figure 7 shows a typical CMOS output with three segments. A certain amount of versatility would be added to a microprocessor/microcontroller if it featured an option to use one, two, or all three segments of output drivers. For high speed, high source/sink current applications, all three segments would be selected. For noise sensitive applications, only one segment would be selected. This selection may be made at the time of fabrication by having a mask option, or, for more versatility, it may be register-programmable.

If the pre-driver of an output is slowed, the transistor switching speed is reduced. This permits slower edge rates and reduced d_i/d_t without compromising current handling capability.

An interesting note is that if transistor sizing is cut down and the pre-driver is slowed, the output slew rate will not be as low as expected. This is because cutting down transistor sizing causes the gate capacitance, Cgs, to decrease. This means the pre-driver is now driving a smaller capacitive load and will turn on faster. This offsets the effect of slowing down the pre-driver response time.

An output transistor with three segments is now considered. The worst case d_i/d_t arises when all three segments are turned on simultaneously. If only the first segment were switched on, the current surge would peak to a relatively lesser value, and then subside. At this time, the second segment could be turned on and finally, the third one. This staggering would restrict noise by distributing d_i/d_t over several stages. The larger number of stages, the less d_i/d_t is. If the output transistor is divided into many stages or subtransistors, and each stage is sequentially turned on, it is known as graded turn-on. Figure 8 shows the equivalent circuit of a distributed transistor (only the n-channel is shown).

The RC network of each subtransistor must charge up before the next subtransistor can turn on. In other words, the RC time constant determines the activation delay between consecutive stages. The physical representation of the distributed transistor is shown in Figure 9a, which shows the conventional transistor where all the segments receive the gate signal simultaneously. The resistors shown in Figure 9b are actually the distributed resistance of the polysilicon.

The problem with graded turn-on is that the turn-off is also slow. For example, if the n-channel is turning on and the p-channel is turning off, the graded switching will cause both transistors to be partially on for quite some time. During this time, a direct path between V_{dd} and ground will result in the device having a high power dissipation. To combat this, the turn-off must be fast and not graded. Figure 10 shows how this is done. The original signal to the distributed transistor is inverted and then used to control the turn-off transistors.

STAGGERED OUTPUTS

On 8, 16, and 32 bit buses, simultaneous switching can be avoided by staggering the outputs (Figure 11). The output enable signals for the drivers are staggered by adding a buffer delay between consecutive outputs. Notably, adding delays introduces a settling time, T_s, after which the data is valid.

CLOCK/OSCILLATOR NOISE

In the case of microprocessors/microcontrollers, much of the radiated noise is from the clock circuitry. Even if the clock signal does not appear at a pin, a considerable amount of clock harmonics may radiate from the oscillator circuit area. To prevent this, the oscillator gain should not be unnecessarily high. To ensure oscillator start-up, a high gain circuit could be used which cuts out once the oscillator is stable.

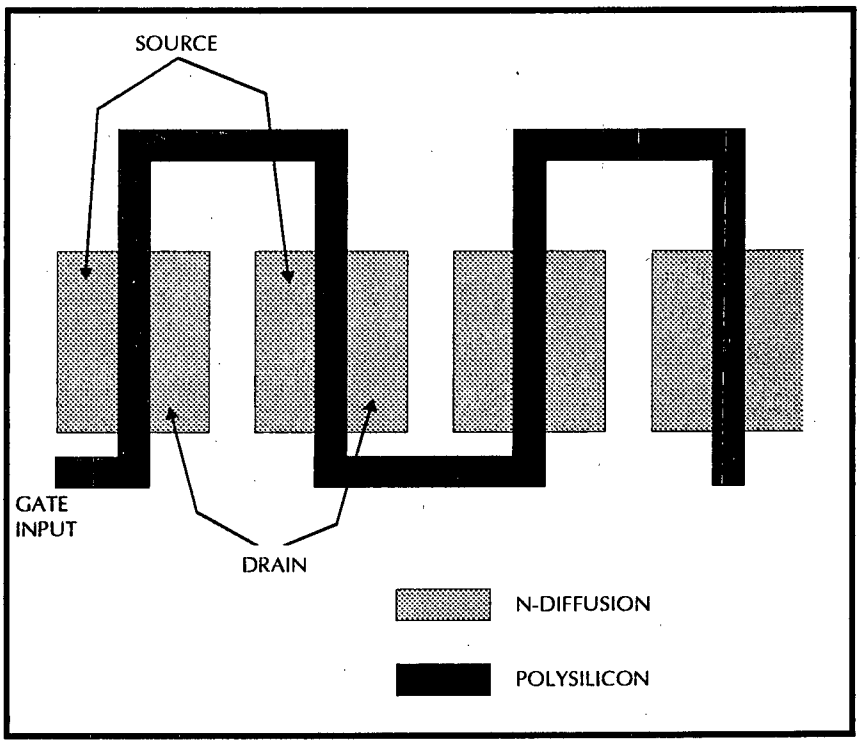

FIGURE 9a. *Serpentine Gate Layout (N-Channel Shown).*

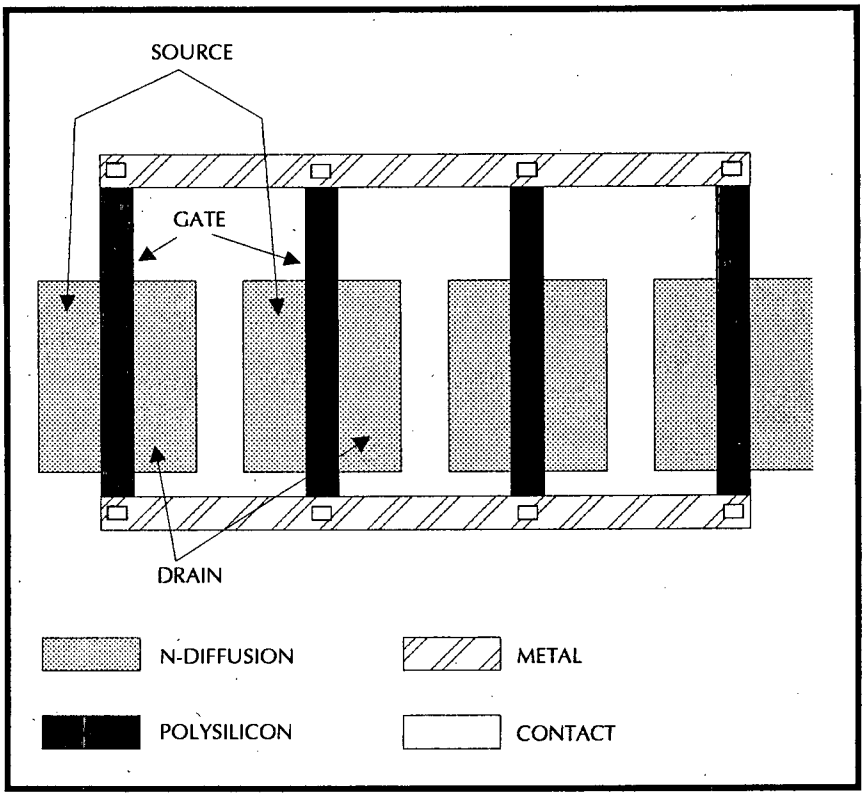

FIGURE 9b. *Conventional Gate Layout (N-Channel Shown).*

CRITICAL DEVICE SPECIFICATIONS

For EMI sensitive applications, the AC/DC product specifications are the most critical factors to consider when selecting

a part. Many systems will malfunction with injected EMI noise. In other applications with analog signals the performance can be greatly degraded. Many factors should be considered:

- Output port drive capability and speed (d_v/d_t) should fit the application. This means that if the load is small, the port should be prevented from switching to fast.

- The number of outputs which can switch simultaneously at any given time is a concern. EMI is cumulative; the more pins switching at the same time, the more energy they will radiate. Outputs that can switch at the same time, like 8 or 16 bit ports, should be "staggered," switching with small delays between each other.

- Repetitive switching outputs, such as pulse width modulators, timer outputs, serial data communication ports, and keyboard scanning ports, should be selected in light of the application. Here it is critical that the frequency used or its harmonics do not interfere with the system. For example, in audio applications the target would be above 25 kHz; in RF systems the switching should be done in the lowest possible frequency range.

- Generally, microcontrollers or digital circuitry is relatively insensitive to external EMI injection, but in noisy environments like automotive applications, noise susceptibility is also of importance. Features like watch dogs, oscillator monitors and other protection circuits are rapidly becoming very desirable.

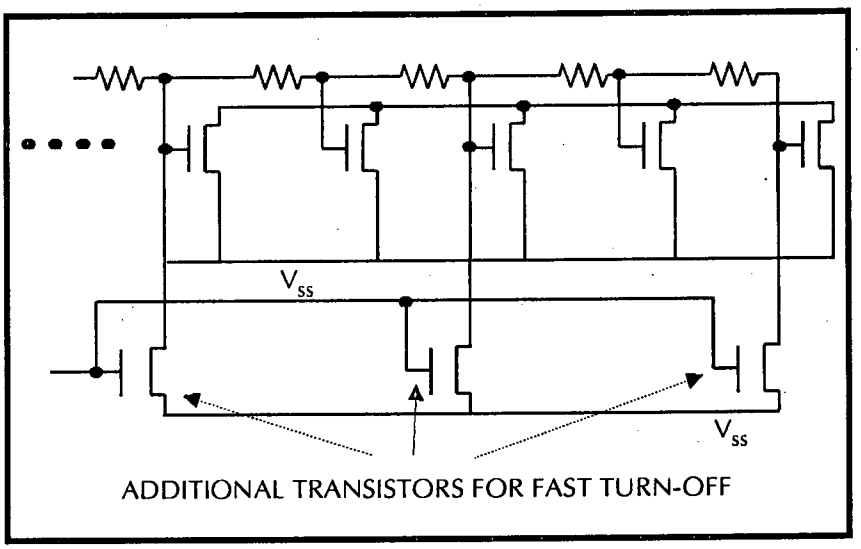

FIGURE 10. *Gradual Turn-on, Fast Turn-off (N-Channel Shown).*

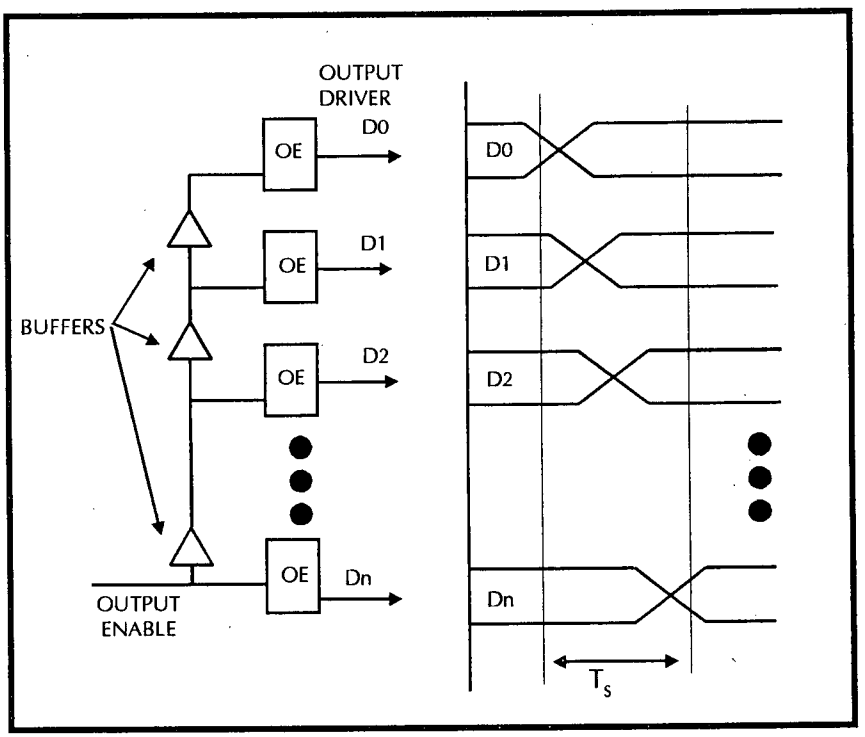

FIGURE 11. *Staggered Outputs and Settling Time, Ts.*

- On-chip oscillators are large contributors to the EMI of a part. The frequency of the oscillator is usually determined by some critical path in the software, for real time control. Therefore, if it is critical that the part is very efficient executing code, it needs an efficient pipeline, short powerful instructions and a register oriented architecture. In this way, the oscillator frequency can be kept low but still achieve a high throughput.

- Maintaining a sine wave oscillation with no clipping is important to reduce the harmonics associated with this. A careful matching of oscillator crystal and capacitors is the key here.

Continued on page 48

- Other good indicators for the EMI performance of a part are operating current, maximum device frequency and minimum operating voltage. These all indicate how fast the device is switching internally. This switching can contribute to the EMI through the ground and power pins of the device. Thus, using a 20-MHz part when 2 MHz is plenty or using 5 V power when the part can work at 3 V is not recommended.

CONCLUSION

Low noise parts clearly give the system designer an edge to offer a better product at an overall lower cost and in a shorter time frame. Clearly, EMC is not just the system designer's problem, but is becoming everyone's concern and should be addressed from logic design through processing, packaging, board and system design.

ANDRE B. WALKER *received a B.S. degree in electrical engineering from Hasselt University, Hasselt, Belgium, in 1986. He is presently working as a senior design engineer in the microcontroller design group at Zilog, Inc. Mr. Walker is a member of the Electrical Engineering Institute of Europe and has published a series of articles on electromagnetic interference. (408)370-8000.*

ANJAN SEN *is a microcontroller design engineer at Zilog. His work has involved the reduction/suppression of EMI in microcontrollers, and he has published a series of articles on EMC. Anjan holds a BSEE from California State University, Chico and is currently pursuing his MSEE at Santa Clara University. (408)370-8000.*