Printed Circuit Board Suppression Concepts for EMC Compliance

PART 1

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This two-part article presents fundamental EMC concepts related to implementing suppression techniques for EMC compliance into printed circuit boards (PCBs). Part 1 appears in this issue of ITEM. Part 2 will be published in ITEM Update, 1998. Together these related articles create one comprehensive document. Both articles present reasons why and how EMC exists within a PCB, along with various design and layout techniques that are easy to incorporate. These design and layout techniques represent a fundamental approach to RF suppression during layout and at the beginning of a design project to minimize EMC threats. Topics examined in the next article will include routing clock traces, impedance control, trace termination, and alternate suppression layout techniques.

Introduction

In today's international marketplace, products must conform to a host of regulations, standards and requirements mandated by government agencies, private standards organizations, and voluntary councils. Mandatory compliance requirements exist for North America, the European Union (EU), and numerous countries worldwide. These regulations cover EMC and essential requirements for product safety.

It is more cost-effective to use design and layout techniques for suppression of EMC within a printed circuit board (PCB) than to rely upon containment measures provided by a metallic enclosure. Top covers, filler panels, I/O adapter brackets, and the like can be removed or damaged by the end user. Sometimes, these items are not designed or manufactured correctly. A system must maintain compliance to EMC standards for as long as the unit provides an intrinsic function to a user. Containment cannot be relied upon for lifetime protection, whereas suppression is always there.

Three elements must be present for EMI to exist. These three elements are: noise source, propagation path, and susceptor. Noise source on a PCB relates to frequency-generating circuits, component radiation within a plastic package, ground bounce, electrically-long trace lengths, poor impedance control, cable interconnects, and the like. Propagation path refers to the medium that carries the RF energy, such as free space or a metallic interconnect. Susceptor is the device which receives undesired RF interference. If one of these three elements is removed, an EMI event cannot exist. It is our task to determine which of the three is the easiest to eliminate. We have no control over the susceptor, as we generally do not know what the susceptor will be. Suppression affects noise source, and is the easiest of the three to implement.

A product must be designed for two levels of performance: one to minimize RF energy leaving an enclosure (referred to as emissions), and the other to minimize the amount of RF energy entering the enclosure (to ensure immunity). When dealing with emissions, a general rule of thumb applies: *The higher the frequency, the greater the likelihood of a radiated coupling path; the lower the frequency, the greater the likelihood of a conducted coupling path.*

Five major considerations exist for EMC analysis, (referred to as "FATID" by Bill Kimmel and Daryl Gerke)[1]:

- *Frequency.* Where in the frequency spectrum is the problem observed?
- *Amplitude.* How strong is the source energy level, and how great is its potential to cause harmful interference?
- *Time.* Is the problem continuous (clock signals), or does it exist only during certain cycles of operation (e.g., disk drive write operation or network transmission)?
- *Impedance.* What is the impedance

of the source and receptor along with the impedance of the transfer mechanism between the two?

- *Dimension.* For transmission of RF energy to occur, an antenna is needed. The physical dimensions that exist, based on trace length or slots within an enclosure determine which particular frequencies are most likely to be observed.

How does RF energy get created within a PCB? Maxwell's equations, derived from Ampere's Law, Faraday's Law, and Gauss's Law describe the relationship between electric and magnetic fields. These equations describe the field strength and current density within a closed loop environment, details of which are beyond the scope of this article.

To oversimplify Maxwell, we relate his four equations to Ohm's Law. The presentation that follows is a simplified approach that allows one to visualize Maxwell in terms that are easy to understand. Although not mathematically perfect, this approach is useful in presenting Maxwell to non-EMC engineers or those with minimal exposure to PCB suppression concepts and EMC theory.

Ohm's Law: $V = I \bullet R$

Maxwell Made Simple:

$$V_{RF} = I_{RF} \bullet Z$$

where

V = Voltage
I = Current
R = Resistance
Z = Impedance (R + jwx)
RF = Radio frequency energy

Comparing *Maxwell Made Simple* to *Ohm's Law*, when RF current exists in a transmission line (PCB trace), which has a fixed impedance value, an RF voltage will be created that is proportional to the RF current. Notice that in the electromagnetics model, R is replaced by Z, a complex number which contains two components: resistance (R, a real component) and reactance (a complex component). For this transmission line example, capacitance does not exist. Each and every trace has a finite impedance value. The inductance that exists within a transmission line (trace) is one of several parameters that allows RF energy to be created within a PCB. The bond wires that connect a silicon die to its mounting pad may also be sufficiently long to add lead length inductance to the trace and to cause EMC concerns. Traces routed on a PCB can be highly inductive, especially traces that are physically long in routed length.

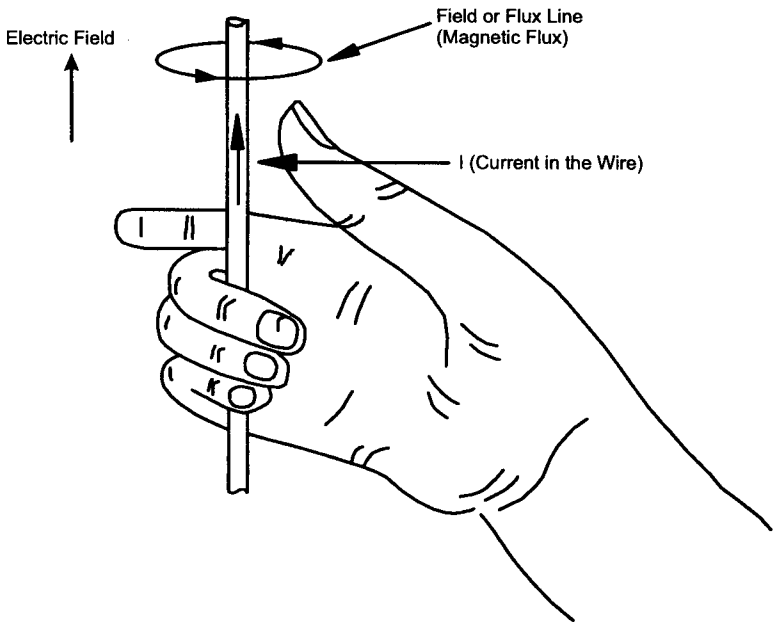

Figure 1. *Right Hand Rule.*

Returning to Maxwell, a moving electrical charge in a transmission line (trace) creates a magnetic field. Magnetic fields created by this moving electrical charge are identified as magnetic lines of flux. Magnetic lines of flux can easily be visualized using the Right Hand Rule (Figure 1). To observe this rule, make a loose fist with your right hand and point your thumb straight out. Current flow is in the direction of the thumb (upwards), simulating current flowing in a wire or PCB trace. Your curved fingers encircling the wire point in the direction the magnetic flux lines (field) travel. This magnetic flux creates a transverse electromagnetic field, commonly called the electric field. The mathematical relationship between magnetic and electric fields is beyond the scope of this article, however, readers should understand that RF emissions are a combination of both magnetic and electric field components. These fields will exit the PCB structure by either radiated or conductive means.

Note that a magnetic field must travel around a closed loop boundary. In a PCB, RF currents are created by a source driver and transferred to a load through a transmission line. RF currents must return to their source through a 0-V reference return system. As a result, a current loop is developed. This loop does not have to be circular, and is often a convoluted shape. Since we must have a closed loop circuit for operation, a source to load and its return path, a magnetic field is developed. This magnetic field creates a radiated electric field. Magnetic fields are typically observed with loop antennas in the near field ($\lambda/4$ of the frequency present), while electric fields are generally observed in the far field ($>\lambda/4$).

Another simplified explanation of how RF exists within a PCB is shown in Figure 2. Here we see a circuit diagram in both the time and frequency domains. A closed loop circuit must exist

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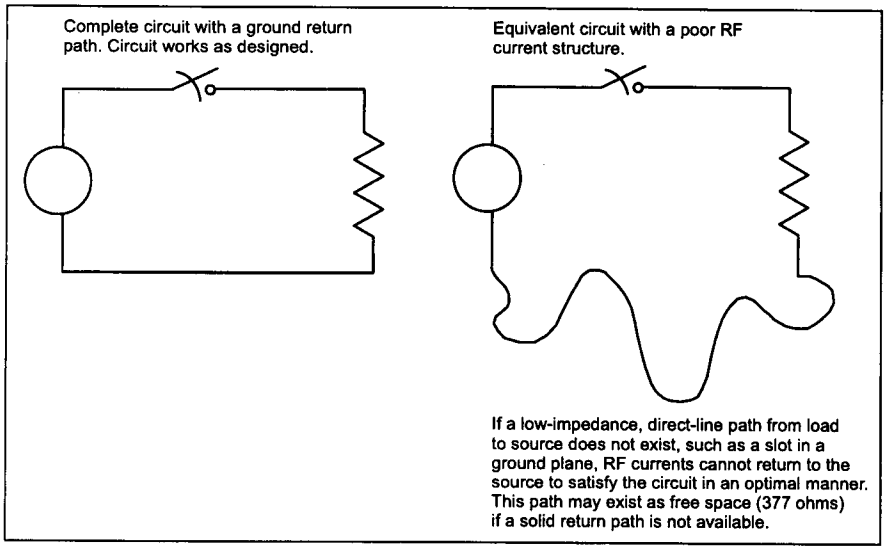

Figure 2. *Circuit Representation - Time and Frequency Domain.*

if the circuit is to work. When the switch is closed, the circuit is complete, and AC or DC current flows (time domain). In the frequency domain, replace the time domain current (AC/DC) with RF current. The RF return path (frequency domain) from load to source must also exist or the circuit would not work. Hence, a PCB structure in both time and frequency domain must conform to Maxwell's equations, Kirchoff's and Ampere's law.

Return currents must travel through a 0-V reference structure (power supply return system), generally a ground trace or ground plane. When RF return current travels from load to source through a planar structure, this path is commonly called an image plane, reference plane or image return path. It is desirable to have the return path located as close as physically possible to the routed trace, discussed later. Because there is a finite, physical distance between the trace and the RF current return path, flux coupling between the magnetic field and the return structure will approach, but not quite reach 100%. *This finite amount of leftover RF current which is not coupled to a return structure is a primary cause of EMI within the PCB.*

Knowing one reason how RF energy is created within a PCB (generation of magnetic lines of flux from a trace), it becomes the designer's job to prevent this residual energy creation. The process of removing unwanted RF currents is called *flux cancellation.* In this author's opinion, flux cancellation is the most important design and layout requirement for RF suppression. The PCB must be designed for use in both the time and frequency domain. Regardless of how well a PCB is designed, both magnetic and electric fields will always exist. If magnetic flux is canceled, EMI cannot exist. It is that simple!

How do we *cancel the flux?* This is easier said than done. Recommendations for layout techniques include, but are not limited to:

- Assign proper stackup and impedance control for multilayer boards.
- Route clock traces adjacent to a 0-V reference plane (multilayer PCB) or use a ground or guard trace (single- and double-sided boards).
- Couple magnetic flux created internal to a component package into the 0-V reference system to reduce component radiation.
- Carefully choose logic families to minimize RF spectral distribution and trace radiation (use slower edge rate devices if possible).
- Reduce RF drive currents on traces by reducing the RF drive voltage from a clock generation circuit, e.g., TTL vs. CMOS drive levels.
- Reduce ground noise voltage within the power and ground plane structure.
- Provide sufficient decoupling for components when all device pins switch simultaneously under maximum capacitive load.
- Properly terminate clock and signal traces to prevent ringing, overshoot and undershoot (enhances signal quality).
- Use data line filters and common-mode chokes on selected nets.
- Properly use bypass (not decoupling) capacitors when external I/O cables and interconnects are provided.
- Provide a grounded heatsink for components that radiate large amounts of common-mode RF energy internal to the device package.

Image Planes and Stackup Assignments

Within a PCB, RF energy is created based on Maxwell's equations. Maxwell describes the existence of both electric charges and magnetic fields. In addition to Maxwell, Kirchoff's and Ampere's laws describe the operation of a circuit or network. Kirchoff's voltage law states that the algebraic sum of the voltage around any closed loop path in a circuit must be zero. Ampere's law describes the magnetic induction at a point due to given currents in terms of the current elements and their positions relative to that point.

If a circuit is to operate as intended, a closed loop network must exist. Figure 3 illustrates a typical circuit. When a trace goes from source to load, return current must also be present, as required by both Kirchoff and Ampere. When the switch is closed, the circuit operates as desired. When the switch is opened, nothing happens. This on/off condition exists for both time and frequency domains. For the time domain, the desired signal travels from source to load and returns through a return path (Kirchoff's Law). In the frequency domain, RF current

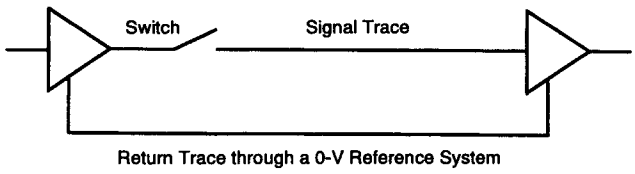

Figure 3. *Closed Loop Circuit.*

must also travel from source to load and return by the lowest *impedance* path possible.

To eliminate undesired RF currents within a PCB (AC signal in nature, while the signal of interest is at a DC potential level) two important words need to be discussed: flux cancellation. If we cancel unwanted magnetic lines of flux, then radiated or conducted RF currents cannot exist. The concept of implementing flux cancellation is simple; however, one must be aware of many pitfalls and oversights that can occur when implementing flux cancellation techniques. With one small mistake, many additional problems will develop for the EMC engineer to diagnose and debug.

Before a detailed discussion of how return planes work is presented, common-mode (CM) and differential-mode (DM) currents are examined. Figure 4 illustrates CM and DM currents as they exist within a PCB.

In Figure 4, current source I_1 represents the flow of RF current from source E to load Z. Current flow I_2 is RF current observed in the return path. RF energy from common-mode currents is the sum of I_1 and I_2. For differential-mode RF currents, the field component is the difference between I_1 and I_2. If $I_1 = I_2$ exactly, differential-mode RF currents will not be present; hence, EMI will not exist. This occurs if the distance separation between I_1 and I_2 is electrically small. Common-mode currents are the main source of EMI. Differential mode currents are rarely observed as a radiated electromagnetic field.

An RF current return path is best achieved with an optimal (low impedance) return path. RF return current will approach zero (flux cancellation). However, if the return path is not provided through a path of least impedance, residual common-mode RF currents will be created. There will always be a finite amount of common-mode currents in a PCB trace since a physical, finite distance spacing will be present between the signal trace and return path (flux cancellation approaches 100%). The portion of the differential-mode return current that does not get canceled out becomes residual RF common-mode current.

The objective in a PCB layout is to have minimal impedance in the RF current return path. If we have a low impedance return path, differential-mode RF currents will be also be minimized. An example of a return path is shown in Figure 5. A multi-layer board with solid power and ground plane provides for excellent flux cancellation. Ground traces usually do not provide optimal flux cancellation under certain conditions. This is because the distance spacing between a clock trace and a ground trace may be physically greater than the distance spacing between the clock trace and the RF reference return plane.

For a reference plane to be effective, *no traces can be located in this solid plane.* Violations can exist only when a PCB layout designer understands how to accommodate this violation using specialized routing techniques. If a signal trace, or even a power trace (e.g., +12-V trace in a +5-V plane) is routed in a solid plane, this solid plane becomes fragmented into smaller parts. Provisions have now been made for an RF signal return loop to exist. Magnetic fields are propagated by loop antennas. This loop occurs by not allowing RF current in the signal trace to seek a straight line path (low impedance) back to its source. Split planes can now no longer function as a optimal return plane to remove RF currents.

A plane violation occurs when a clock trace is routed over a moated area. A moat is an absence of copper on all power and ground planes of a PCB. If a trace is routed over a moat, the RF current return path is not direct back to the source, and an RF current loop will be created causing radiated EMI. This is detailed in Figure 6.

Common-mode RF currents are generally observed in I/O interconnects. Rarely is common-mode noise observed

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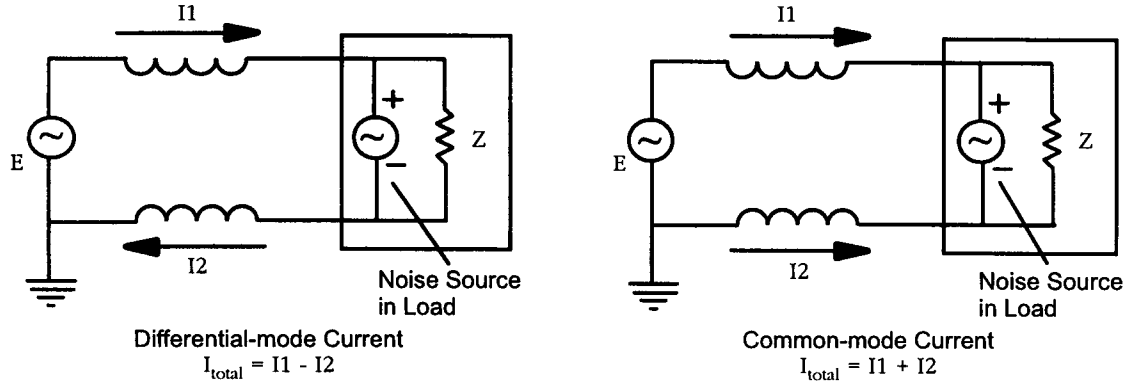

Figure 4. *Common- and Differential-mode Configurations.*

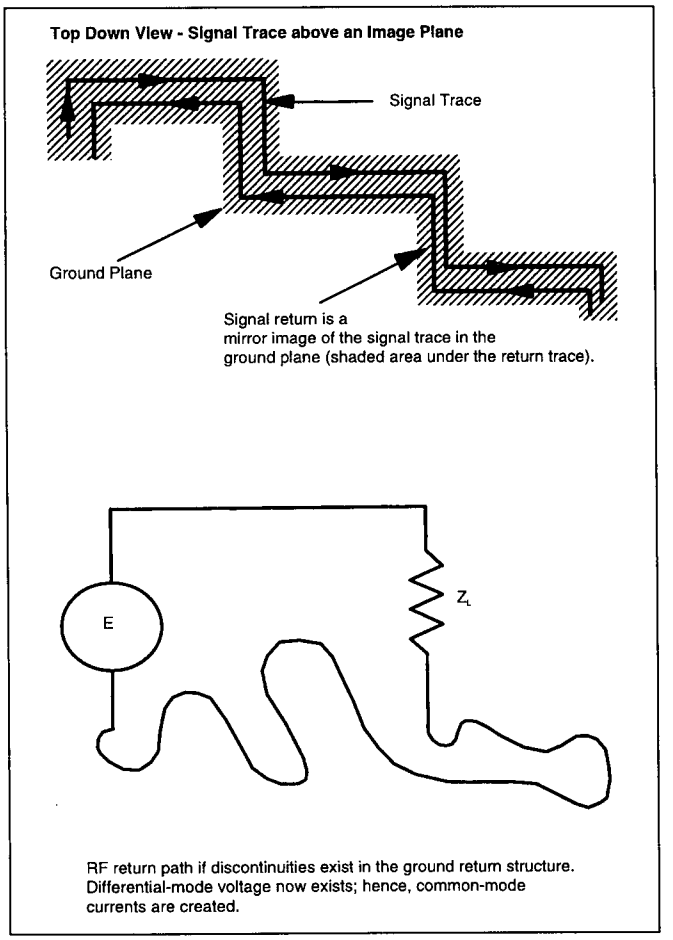

Figure 5. *Image Plane Concept.*

internal to the PCB. Differential-mode currents can also be created as a result of a voltage gradient IZ drop that occurs between two points sharing the same 0-V reference. With an IZ drop, ground noise voltage is induced between these two circuits.

To implement flux cancellation within a PCB using reference planes, it becomes mandatory that critical nets with large RF spectral energy be adjacent to a solid RF return plane, preferably at 0-V (ground) potential. Ground planes are preferred over power planes because various logic devices may be quite asymmetrical in their pull-up/pull-down current ratios. These switching components may not present an optimum condition for flux cancellation due to signal flux phase shift, greater trace inductance, poor impedance control and noise instability. The ground plane is also preferred because this is where heavy switching currents are shunted. TTL asymmetric drive is heaviest to ground, with less current spikes to the power plane. For Emitter Coupled Logic (ECL), the more noisy current spikes are to the positive voltage rail. For CMOS, both power and ground reference are equal.

Examples of typical stackup assignments are shown in Figure 7. Stackup assignments for specific designs will be different due to the number of routing layers, power and ground planes required, or special engineering design requirements. Adjacent to each 0-V reference (ground) plane is a signal routing plane that must contain all clocks and other traces rich in RF energy.

Generally, a one- or two-layer PCB will not contain a ground or 0-V reference plane. As a result, optimal flux cancellation cannot occur. For a single- or double-sided stackup, each clock trace or sensitive circuit must be completely surrounded by a separate trace at 0-V reference potential. This 0-V reference trace must be connected to the 0-V reference from the power supply. The ground trace must also be located as close to the signal trace as physically possible based on the manufacturing process used to fabricate the board. This ground trace thus provides an alternate return path for RF currents to return to their source if a solid ground plane is not provided.

Bypassing and Decoupling

Capacitors are used for various functions within a PCB. Some of these functions include minimizing ground bounce, shunting RF energy between functional areas and I/O interconnects, and removing common-mode and differential-mode RF currents from a circuit. Capacitors not only prevent RF emissions from being created, they assist in minimizing externally-induced RF fields from entering the product (immunity protection). Before we examine how capacitors work, a definition of three different uses for capacitors is provided. Capacitors are used in one of three configurations; decoupling, bypassing and bulk.

Decoupling capacitors remove RF energy generated from high frequency switching components. They provide a localized source of DC voltage for devices or components, and are particularly useful in reducing peak current surges from being propagated across the PCB.

Bypassing capacitors remove unwanted RF noise that couples component or cable common-mode EMI into

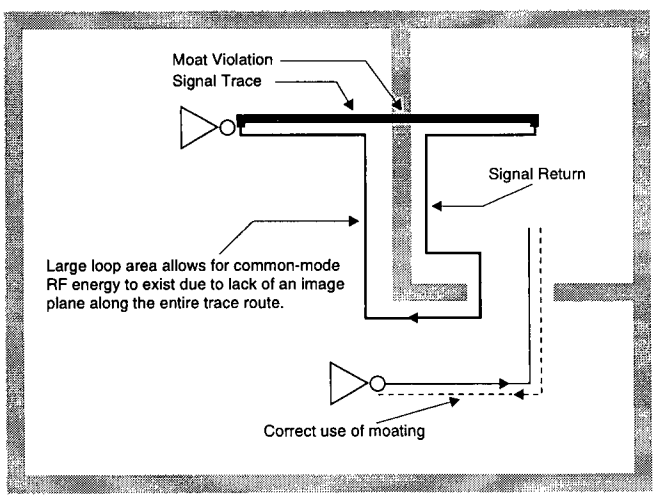

Figure 6. *Moating Concept.*

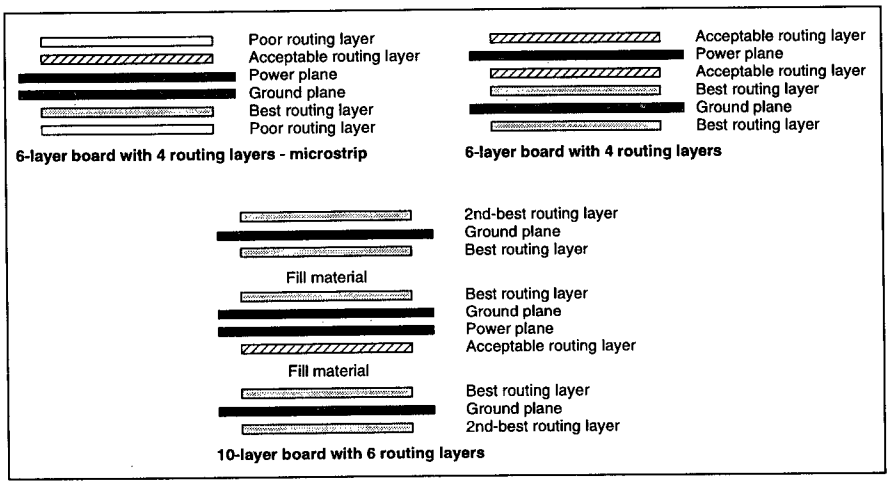

Figure 7. *Sample Stackup Assignments.*

susceptible areas. They also provide other functions of filtering, as they are bandwidth limited.

Bulk capacitors maintain constant DC voltage and current to components when all signal pins switch simultaneously under maximum capacitive load. Bulk capacitors prevent power dropout due to dI/dt current surges generated by components consuming voltage and current within the power distribution system.

Restated, bypassing and decoupling refers to the prevention or propagation of RF energy from one area to another. These areas are power and ground planes, components, and internal power connections to I/O connectors. Bulk capacitors provide DC power to components to prevent a momentary voltage drop from occurring when a power supply is not located in the vicinity of the switching device.

Decoupling provides a localized source of charge for the proper operation of components during clock or data transitions, especially when all signal pins switch simultaneously under maximum capacitive load. Decoupling is accomplished by ensuring there is a low-impedance power source present in the power distribution system. Because decoupling capacitors have decreasing impedance (ability to remove RF switching currents) as the frequency increases up to the point of the capacitor's self-resonant frequency, high frequency noise is effectively removed from the power distribution system while low frequency RF energy remains relatively unaffected. All capacitor values and dielectric material must be chosen based on desired performance; they cannot be left to random choice from past usage or experience.

Capacitors consist of an *LCR* circuit with *L* (inductance in the lead length), *R* (resistance in the leads) and *C* (capacitance). A schematic representation of a capacitor is shown in Figure 8. At a known frequency, the series combination of *L* and *C* becomes resonant, providing very low impedance and effective RF shunting at resonance. At frequencies above self-resonance, the impedance of the capacitor becomes increasingly inductive and bypassing or decoupling becomes ineffective. Hence, the lead lengths of capacitors (surface mount, radial or axial), including trace length between a component and the capacitor, vias in the circuit, and the like, affect operational performance. Lead length inductance is an important parameter to consider when selecting capacitors for bypassing and decoupling. Other important parameters are the dielectric material and the tolerance rating of the capacitor.

If a capacitor must be used for a particular application, the question that exists is how to properly select this capacitor and how to incorporate it into the design.

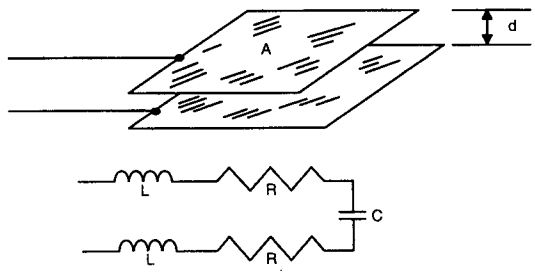

Figure 8. *Physical Characteristics of a Capacitor.*

DECOUPLING CAPACITORS

Components that switch logic states must be RF decoupled. This is because the switching energy generated by logic components will be injected into the power distribution system. This switching energy will be transferred to other logic circuits or subsections as common-mode and/or differential-mode RF noise. Typically, one selects a capacitor with a self-resonant frequency in the range of 2 - 100 MHz for circuits with edge rates of 2 ns or less (slower speed components). Typical multilayer PCBs are self-resonant in the 150 - 300 MHz range. Proper selection of decoupling capacitors, along with knowing the self-resonant frequency of the PCB assembly (acting as one large bulk capacitor) will provide enhanced EMI suppression of digital switching noise. Surface mount devices have a higher self-resonant frequency by up to two orders of magnitude (or 100). This higher self-resonant frequency is due to less lead length inductance. Aluminum electrolytic capacitors are ineffective for high-frequency decoupling and are best suited for power supply subsystems or power line filtering.

In addition to bypassing, high-frequency RF decoupling must always be provided in all clock generation areas. To do this, calculate the decoupling capacitance

value to suppress RF switching noise for all significant clock harmonics. Choose a capacitor with a self-resonant frequency higher than the clock harmonics requiring suppression, generally considered to be the fifth harmonic of the original clock frequency. In addition to this selection criteria, one must be cognizant of the amount of energy the capacitor provides to the component for proper operation.

Decoupling capacitors ideally should be able to supply all the DC current necessary during a state transition. Calculation of the local point-source charge of the decoupling capacitor is represented by Equation 1. This equation does not calculate self-resonant frequency, only the localized source charge required to remove RF switching noise from the power distribution system. As observed, use of 0.1-µF capacitors in today's products are usually insufficient for optimal decoupling when the edge rate of the device is faster than 5 ns. Use of decoupling capacitors on two layer boards is, however, required to reduce power supply ripple. Decoupling capacitors for low frequency applications are usually not needed when multilayer boards are used, given that the capacitance between the power plane and ground planes provides overall decoupling for low frequency or slower edge rate components and are more efficient than discrete components.

$$C = \frac{\Delta I}{\Delta V / \Delta t} \qquad (1)$$

$$\text{i.e., } \frac{20 \text{ mA}}{100 \text{ mV} / 5 \text{ ns}} = 0.001 \text{ µF or } 1000 \text{ pF}$$

where
C = Capacitance
I = Current transient
V = Allowable power supply voltage change (ripple)
t = Switching time

When selecting decoupling capacitors, in addition to providing a localized source charge, calculate the self-resonant frequency based on the actual edge rate of the logic family used, not a manufacturer's data book value; the real, unpublished edge rate. Equation 2 provides for calculating the self-resonant frequency of a capacitor. Be aware that inductance is a part of this equation. Lead length inductance is not intuitively known, and is usually an unknown constant.

$$\omega = 2\pi f = \sqrt{\frac{1}{LC}} \qquad (2)$$

A capacitor remains capacitive up to its self-resonant frequency. Above self-resonance, the capacitor becomes inductive and ceases to function for RF decoupling. This is observed in Figure 9. Placement of the capacitor should also be as close to the component pin as physically possible to minimize lead length inductance if a multilayer board is not provided. It is common practice to use a 0.1-µF capacitor for decoupling high technology PCBs which is a poor choice in today's high-technology, high-speed systems. This 0.1-µF value was selected in 1965 by the USA military to decouple 20-kHz components. Components used in today's products now require decoupling in the range of 0.01-µF to 100 pF. Again, capacitance value and lead length inductance determines the self-resonant frequency and the amount of decoupling provided.

Another concern for selection of a decoupling capacitor is the dielectric material used to manufacture the device. Figure 9 shows the self-resonant plots of three different dielectric materials. The cost of using specific dielectrics is negligible, especially when EMI compliance is required and decoupling will assist in solving the emissions problem.

A benefit of using multilayer PCBs is the placement of the power and ground planes adjacent to each other which creates one large decoupling capacitor, generally in the range of 150-300 MHz. This internal decoupling capacitor usually provides adequate decoupling for slow speed (slow edge rate) designs. If components have signal edges (*tr*) slower than 10 ns (e.g., standard TTL logic), use of low, self-resonant frequency decoupling capacitors is generally not required as the majority of decoupling is performed by the internal power and ground planes. Bulk capacitors, however, are still needed to maintain proper voltage levels for performance reasons. Above the upper limit of decoupling provided by the power and ground planes, discrete capacitors must still be used for operation above 300 MHz.

BYPASS CAPACITORS

Bypass capacitors are commonly used to divert common-mode RF currents that are present on cable shields by creating an AC short to chassis ground. RF currents are, in reality, an AC component (sine wave). Bypass capacitors must be placed where I/O interconnects attach to the PCB. If the braid of the cable is floating, or not bonded to chassis

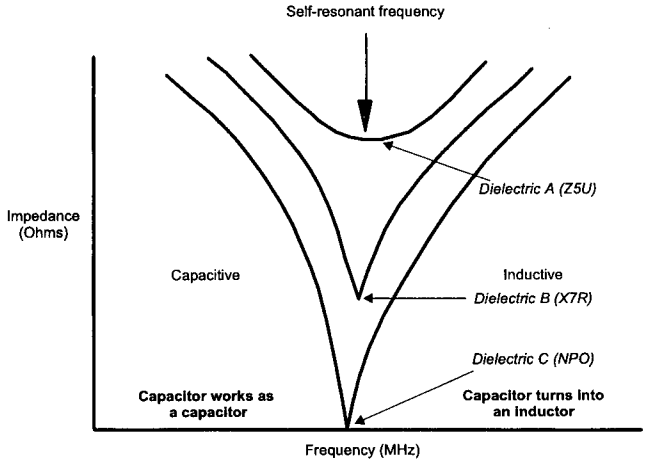

Figure 9. *Dielectric Material and Self-resonant Frequency of Same Value Capacitors.*

ground, a bypass capacitor is required to remove common-mode currents present on the cable shield from either radiating into free space or causing a disruption to the chassis due to an immunity event. Again, short lead lengths are a primary design consideration. When selecting bypass capacitors, proper bandwidth filtering and peak surge voltage protection capabilities for electrostatic discharge (ESD) protection should be kept in mind.

Another item to remember for ESD protection is to use bypass capacitors with a high self-resonant frequency between the power and ground structure. These bypass capacitors must have as low an equivalent series inductance (ESL) and equivalent series resistance (ESR) as possible. Frequent use of bypass capacitors reduces loop areas between the power and ground planes for low-frequency, high-level ESD events. For higher-frequency ESD, standard value capacitors (i.e., 0.1 μF) become less effective due to both the capacitors' internal stray and interconnect trace inductance to the component or ground stitch location. Use of MOVs, transient suppression devices, spark gaps, diodes, etc., may also be required.

BULK CAPACITORS

Bulk capacitors maintain proper dc voltage and current to components when these devices switch all data, address and control signals simultaneously under maximum capacitive load. Large power consuming components will cause voltage fluctuations on the power distribution system. These fluctuations will cause improper circuit performance due to voltage sags, ground bounce and ground noise voltage. Bulk capacitors also provide large amounts of energy storage to maintain voltage and current requirements of switching components. Bulk capacitors play no significant role in EMI control.

Bulk capacitors, usually tantalum dielectric, must be used in addition to higher self-resonant frequency decoupling capacitors to provide DC power for components and to prevent power plane RF modulation. Place one bulk capacitor for every two LSI and VLSI components in the following locations:

- Adjacent to clock generation circuits
- At the power entry connector on the PCB
- At all power terminals on I/O connectors for daughter cards, peripheral devices and secondary circuits
- Near power-consuming circuits and components
- At the furthest location from the input power connector
- High density component placement remote from the DC input power connector

When using bulk capacitors, calculate the capacitor voltage rating such that the nominal circuit working voltage equals 50% of the capacitor's voltage rating to prevent the capacitor from self-destruction if a voltage surge occurs.

Conclusion

When examining how EMI is created in a PCB, various engineering aspects related to Maxwell's equations must be considered. The existence of magnetic lines of flux present within a transmission line structure is the primary cause of RF energy generated within the PCB structure. Other major areas of concern include the creation of common-mode and differential-mode currents between circuits and interconnects, ground loops creating a magnetic field structure between components and ground structures, and component radiation from a device package.

To reduce or eliminate unwanted RF energy, magnetic lines of flux must be removed. This is easily performed using flux cancellation techniques. The most common and easiest method is to provide a return path that is as physically close as possible to the offending transmission path to allow the closed loop circuit to become tightly coupled. This is best accomplished with return planes and traces at 0-V reference. Keeping the RF return path adjacent to the trace containing the flux is mandatory without routing the return path over gaps in the return plane.

One must differentiate between decoupling and bypassing when implementing suppression techniques on a PCB. Decoupling is provided at the component level to prevent ground-noise voltage and high frequency voltage spikes being injected into the power and ground plane structure. Differential-mode voltages create common-mode currents. It is common-mode currents that are measured as EMI emanating from a product. Bypass capacitors divert common-mode currents from I/O cables, thus allowing only the desired data stream to be present. Bulk capacitors keep the unit functioning by insuring that sufficient voltage is present for all circuits under maximum power consumption usage while assisting in preventing ground bounce from occuring.

Reference

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