ELECTROMAGNETIC COUPLING

The coupling theory and computation, although interesting, are often ignored during detailed design work. Generally, the detail of selecting pin location and wire routing is left up to drafting or board designers who have relatively little EMI coupling theory background: Two fundamental design errors are the frequent outcome:

- over-design by separation of conductors with extra connectors adding weight, cost, etc.; and
- under-design, meaning the improper or random selection of pin locations and wiring design, which results in EMI problems.

This article presents a summary of the authors' experience with coupling problems and corresponding test results, in an effort to help designers estimate design margins and minimize the effects of over-design or EMI.

Component I/O Connector Coupling

The interfacing of several classes of circuit types within a single component or enclosure complicates the design of electronic equipment. Circuit classes vary from primary input power to low level digital and analog signals. The design engineer is faced with the decision to separate these classes, using individual input/output connectors or to discretely isolate unlike power and signal classes within common connectors. The decision tradeoff considerations include:

- pin-to-pin coupling levels for EMC and TEMPEST reduction;
- utilization of connectors and panel space;
- environmental leakage; and
- costs.

In addition, designers misinterpret program definitions of EMC circuit classifications. The circuit classes for long harnesses and cables are often applied to the input/output connectors, unnecessarily adding connectors to the equipment design. Use of the multi-class approach can result in a component design where connector pin utilization is not efficient.

Often the subject of debate among designers, the multi-class approach has been resolved by experimental coupling tests on several programs. The results are that separate connectors are not required for components using standard 60Hz or 400Hz, 120 volt AC power and/or 28 volt DC power. Capacitive and/or inductive coupling from these powerlines to sensitive digital or analog circuits can be minimized by proper pin selection and cable separation after passing through the connector.

Type "D"/Connector Coupling Tests[1]

A series of coupling experiments was performed to determine inductive and capacitive coupling characteristics of a typical "D" type Connector interface. The results of these tests are illustrated on Figures 1 and 2. Several user frequencies and pin variations have been tabulated in Table 1. The user is advised that this is coupling in the connector and 1 inch of input/output wiring only.

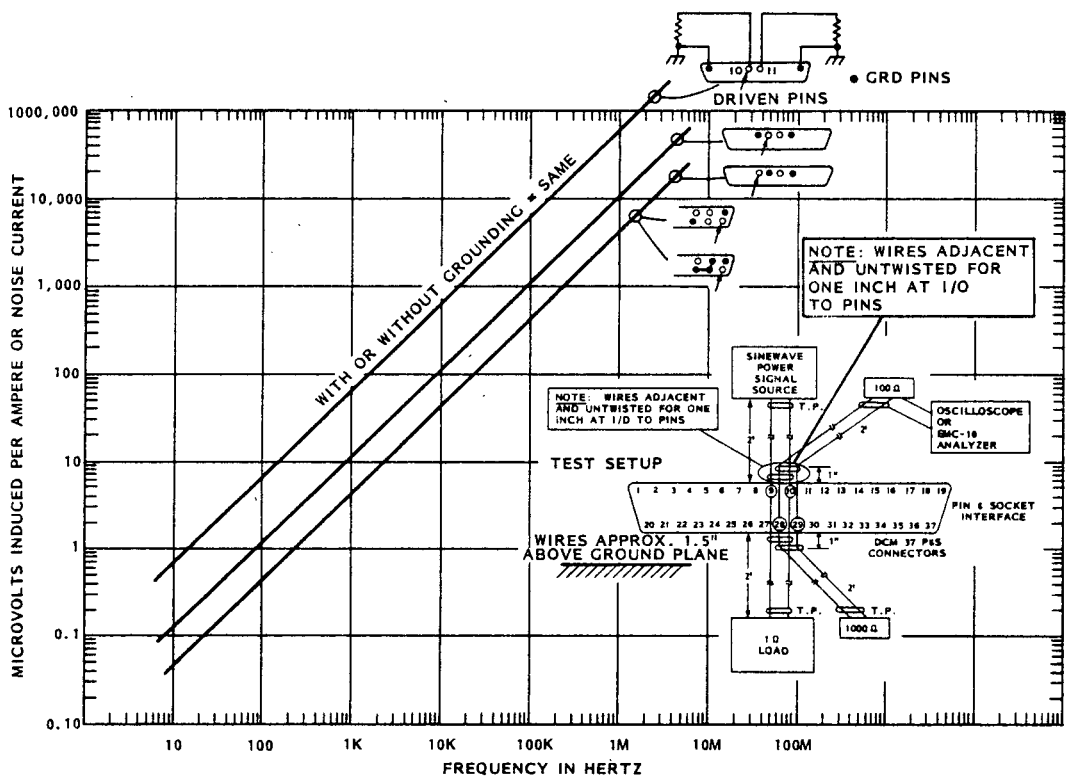


Figure 1. Inductive or Current Caused Coupling within the Cannon DCM-37 P&S Connectors (Mated)

[1]G. P. Condon and J. S. Thompson, "Electromagnetic Coupling and Leakage Within Connectors" Electronic Connector Study Group, Delaware Valley Chapter Meeting, November 1980.

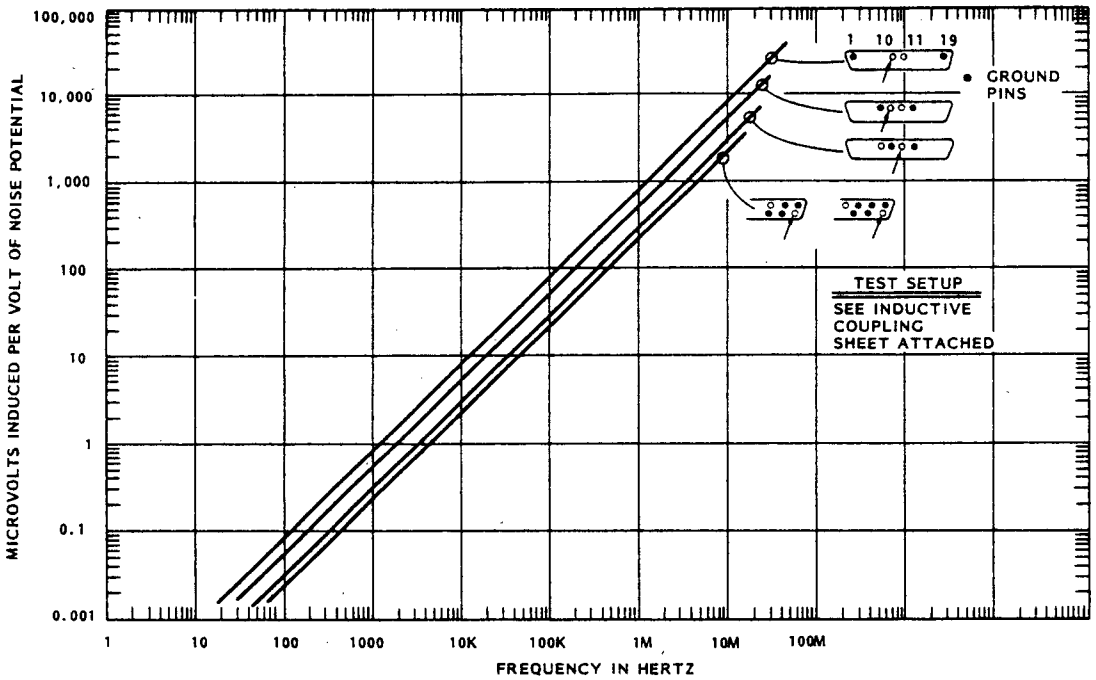


Figure 2. Capacitive or Voltage Caused Coupling within the Cannon DCM-37 P&S Connector (Mated)

Mixing Low Level Balanced Video with Others

Figures 3 and 4 show related experience with low level video (TV) signals and high noise content sweep waveforms. The criteria for a susceptible video level was 5 millivolts p-p. These curves show the maximum voltage and current versus frequency allowable on adjacent pins to just meet the 5 millivolt p-p criteria. Notice that for 20KHz noise with 4 inches of adjacent wire/pin would require 20 amperes p-p and about 300 volts p-p.

Interpretation of test results and the conversion of results to a typical user design guide table is presented in Table 1. The Table illustrates the extent of coupling to be expected for various pin locations with powerlines, digital signals and spikes on pins within the same connector. In the connector diagrams, the circle with the arrow represents the driver or source pin, the other circle represents the pickup or sensitive pin, and the solid dots represent the return pins. The Table illustrates that return pin locations and "guarding" can reduce coupling by over an order of magnitude.

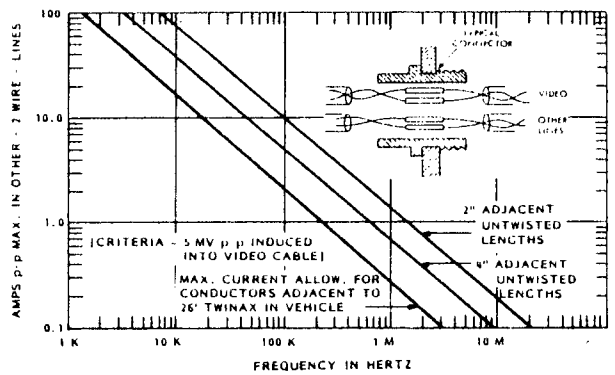


Figure 3. Inductive Coupling—Maximum Current Allowable on Other Two-Wire (Hot and Return) Adjacent Pins within Bendix Connectors

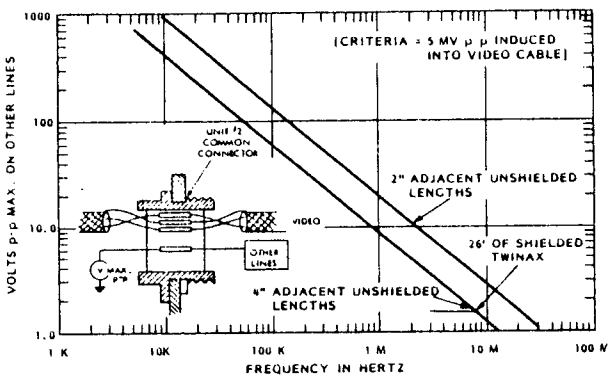


Figure 4. Capacitive Coupling—Maximum Voltage Allowable on Other Pins within Bendix Connectors

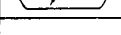
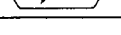
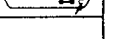
SOURCE	FREQUENCY	PIN LOCATION DM 37 P&S CONNECTOR		
				
POWER	60Hz			
	VOLTAGE	.07μV/V	.04μV/V	0.01μV/V
	CURRENT	4μV/A	0.3μV/A	0.3μV/A
	400Hz			
	VOLTAGE	0.3μV/V	0.2μV/V	0.1μV/V
	CURRENT	30μV/A	6μV/A	2μV/A
	10KHz			
	28V Switchers			
	VOLTAGE	10μV/V	5μV/V	2μV/V
	CURRENT	700μV/A	100μV/A	40μV/A
DIGITAL	2MHz			
	VOLTAGE	2MV/V	1MV/V	0.3MV/V
	CURRENT	10MV/50ma	1MV/50ma	.4mv/50ma
SPIKES	10μS wide	2.3mV/V		
	$t_r \approx 1\mu s$	4mV/A		

Table 1. Typical User Frequencies vs. Pin Location

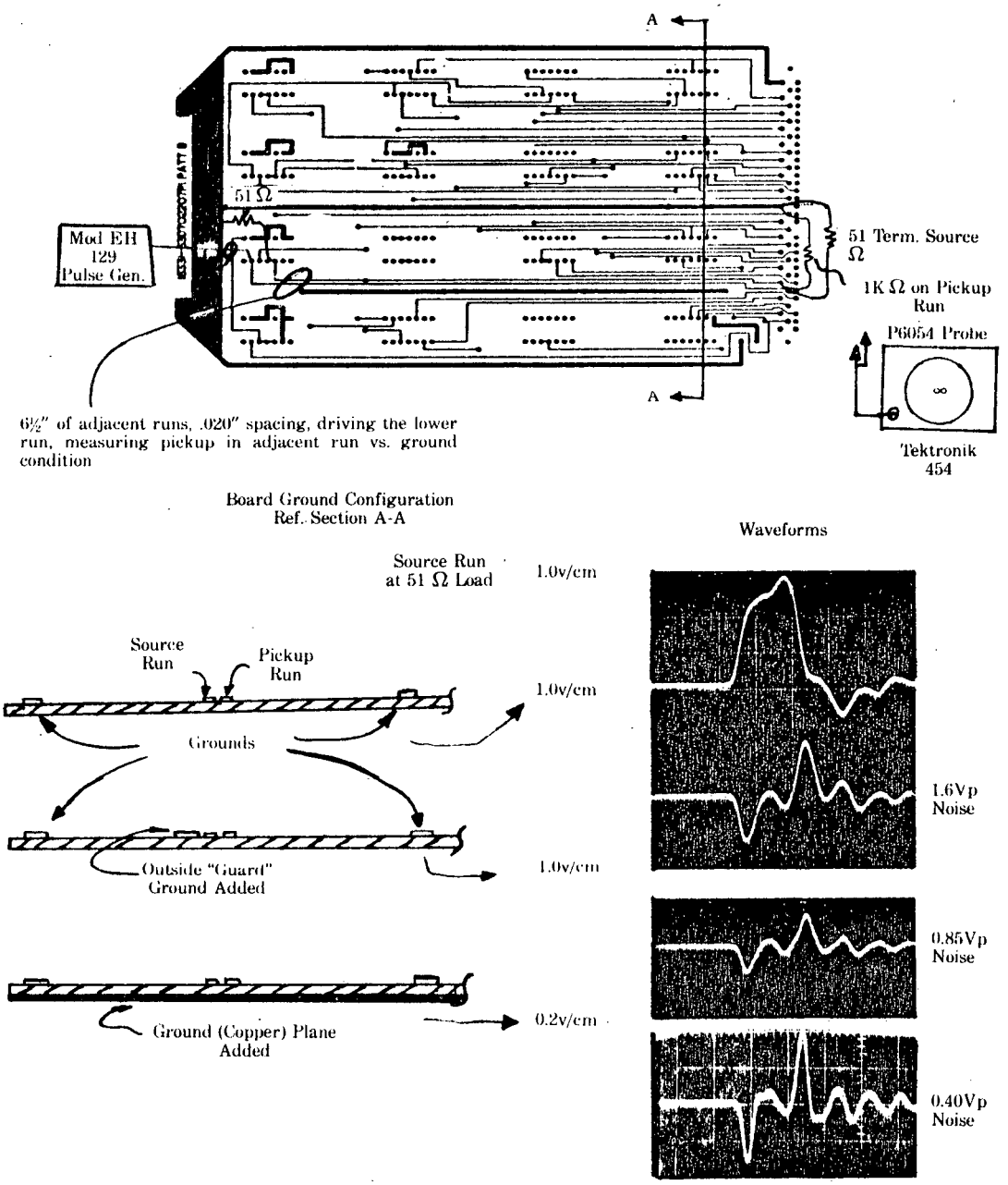


Figure 5. Noise Coupling vs. Grounding Demonstration

P.W. Board Coupling[2]

Logic timing boards operating at 2 to 3 nanosecond switching rates can be in serious trouble due to noise. The boards, containing high speed Schottky timing logic, were laid out on standard two-sided board material using existing design practices. Coupling and common mode ground current on the board produced 1.5 volts of noise. These problems were resolved by redesigning the board's grounding system.

Proper instruction is the secret to designing many different Schottky logic boards. Many draftsmen, and even some logic designers, fail to comprehend that they are dealing with 500 MHz signals and that R.F. strip line design techniques are required.

To accommodate the nonbelievers, a P.W. board was used to demonstrate the problem. A chip location 6.5 inches from the connector was used to drive a run leaving the board. The signal rise/fall time was about 3 nanoseconds. An adjacent run circuit was monitored for coupled noise with various simulated grounding conditions (see Figure 5). The results show that coupling of 1.6 volts exists even when the ground paths are 0.050" runs, only an inch or so away on each side of the tested pair. The 1.6 volts of board run coupling will easily exceed logic gate thresholds of 1.3 and 1.5 volts.

A design guide consisting of 6 basic steps was prepared. The rules were kept simple and straightforward (see Table 2).

Board coupling tests were performed on critical timing boards. The test set up duplicated that mentioned above, i.e., two adjacent runs 6.5" long leaving the board. The new timing boards produced 0.46 volts p-p of coupled 10mHz clock onto the adjacent run. Comparatively, the early version of the board from another program produced 1.6 volts of coupled noise, for similar run conditions.

[2]G. P. Condon, "Solve Two Sided Logic Board Noise Problems the Easy Way, at the Drafting Board," GE GOSAM Conference, 15 December 1976.

Table 2. P.W. Board Grounding Guides

1. I/O Pins—Use five (5) ground pins, equally spaced along the connector, to permit I/O signals to be routed adjacent/nearby ground.
2. Dedicated Board Ground Runs—Connect the five (5) ground pins to ground runs (.050" wide), and run up the board, as equally spaced as possible. These may be staggered to relieve congestion. However, this practice shall be minimal.
3. Clocks and Inputs to Storage Devices—Clock (timing pulses at basic rate or submultiples) should be routed with ground. *Clock should be installed on the board initially with the 5 ground busses prior to other circuit layout. Route the clock on the opposite side of the ground run/buss.
4. Storage devices such as *flip/flops, registers, or other latching type circuits should be treated as special and laid out on the board prior to laying in all other signals. These runs should be routed over ground and "guarded" on the board with adjacent ground or power runs. "Guarding" provides up to 9:1 reduction in capacitance between adjacent runs.
   The board design may then be done as normal. Chip grounds shall be tied continuously to the board's horizontal ground runs. Vertical jumpers .015" wide shall then be added to tie the ground runs together, at each row where space is available.
5. Reexamine the board and use a landfill technique to fill in the open areas with ground plane. Planes/sections will exist on both sides of the board, and they are interconnected with plated-thru holes on their edges/corners wherever possible. If not leave land slices ungrounded; they still reduce coupling and provide a R.F. return path.
6. The completed board should have the following characteristics:
   - When held to the light, the board is almost opaque, due to copper.
   - Chips are referenced together vertically, as well as horizontally.

*Clock signals and F/FS, register inputs, etc., shall be clearly identified by the logic designer on his inputs to Drafting.

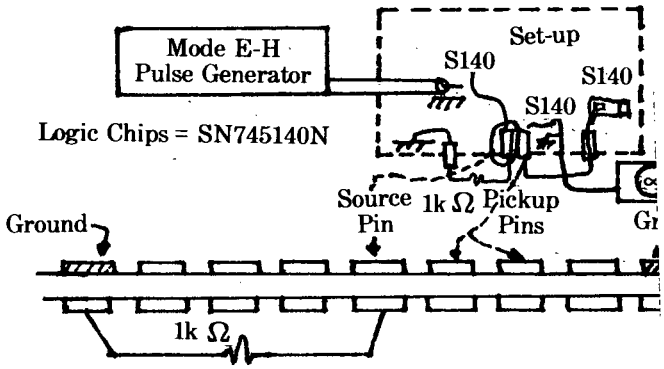
The board design approach has since been factored into the Machine Automated Drafting (MADS) program for new board designs. The MADS Applicon automatically dedicates the grounding system first, then adds clock runs, signal runs and power runs to complete the board.

Adjacent pin coupling adds approximately 0.15 volts to the 0.46 volt adjacent run noise for the worst case pin location between ground pins. Figure 6 illustrates this test configuration and results.

Harness and Wire Wrap Coupling

Coupling of digital signals within common classes of harnesses or cables can also be a problem in digital systems integration. Often designers try to combine single-ended digital signals into common cables whose length exceeds good safety margin. The result from a 20-foot long cable is that digital noise coupling exceeded the 1.3 volt threshold of input logic gate circuits.

Table 3 illustrates expected coupling levels between various wiring configurations commonly used in digital (T^2L) equipment. Note that a 16-to-1 reduction can be achieved using twisted pair wiring, and an 85-to-1 reduction using shielded wire or coax. Also note that for ordinary twisted pair wiring the 1.3 volt threshold may be exceeded for 30 feet of cable, depending on the wire lay in the bundle.



Edge, Pins on 0.1 Inch Centers

Pickup Pin Location	Noise Coupled
1st (Adjacent)	0.15V o-p
2nd	0.10V o-p
3rd	0.05V o-p
Back to Back	0.08V o-p

Test Results

Figure 6. Coupling in the I/O Edge-Board Connector for Ground Spaced 0.8"

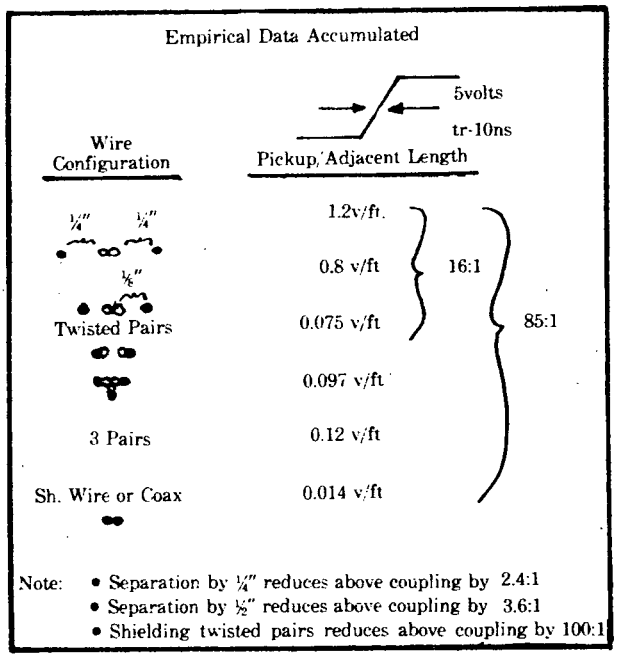


Table 3. Coupling in Digital Harnesses for T^2L Circuits

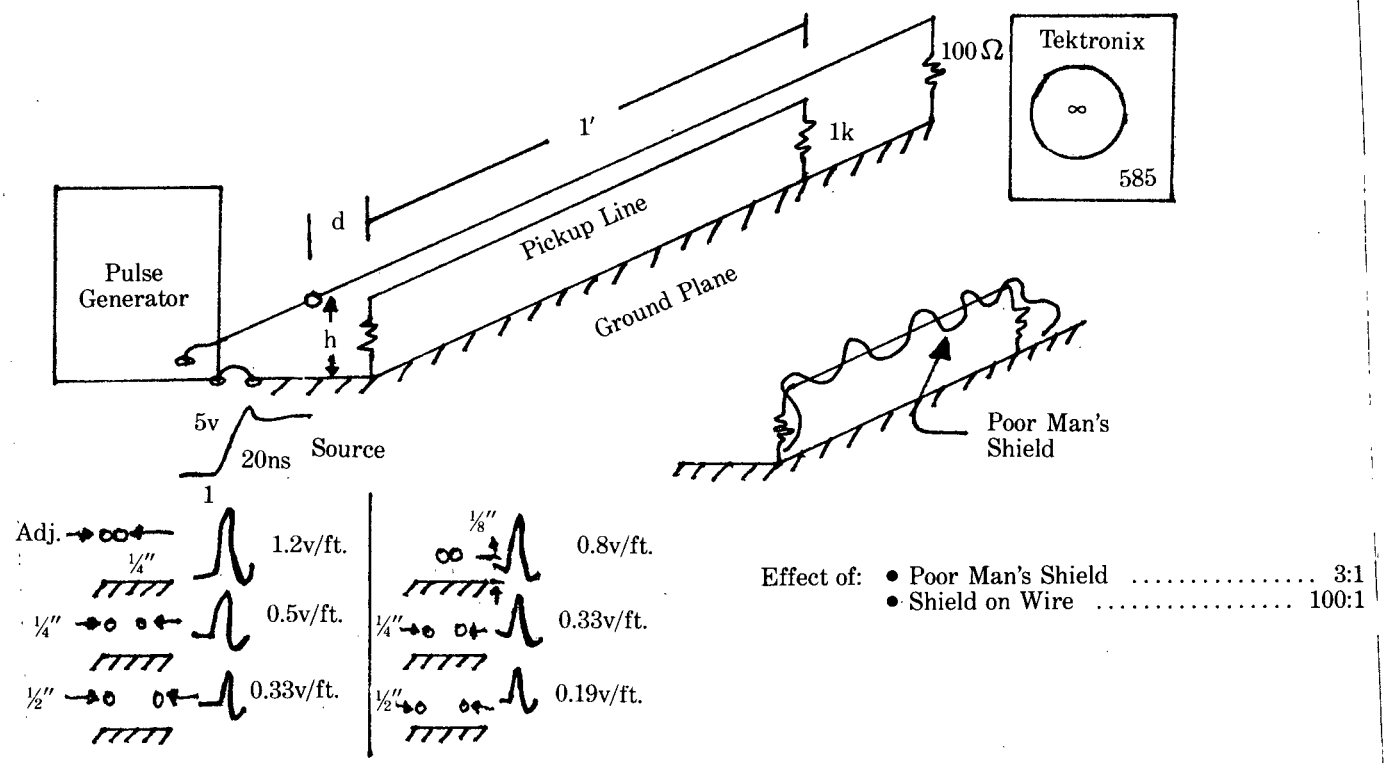


Figure 7. Wire Wrap Coupling for 5 Volt Logic, Above Ground

Coupling of digital signals on wire wrap boards or logic back planes can also be a serious problem. Figure 7 illustrates test data for a variation of wire locations above the board's ground plane. Note that up to 1.2 volts per foot can result where the wires are adjacent and above the ground plane by approximately ¼ inch (i.e., Z_2 level). Separation to ½ inch and use of the Z_1 layer level reduces the coupling to 0.2 volt/foot. Since it is very difficult to know what to separate and which wires to lower to the Z_1 layer for large processing systems, several design guides have been instituted:

1. Never attempt to design high speed logic board or backplane without a ground plane.
2. Either manually or via computer program, analyze the wire lengths and place the longer wires on the Z_1 level, i.e., next to the ground plane.
3. Add shorter lengths to Z_2 or Z_3 levels.
4. Interconnect ground pins together to form an overhead ground grid at the Z_3 level. (This sandwiches the signals between the ground plane and the Z_3 ground grid, minimizing wire-to-wire coupling, and shields the wires to prevent radiation, which could cause non-compliance with EMC Spec. MIL-STD-461 or FCC Docket 20780.)

Conclusions

The physical "minor details" of fabricating digital equipment and systems can grossly affect the electromagnetic compatibility of the item. It is hoped that this article will help designers to anticipate coupling effects early in the design stage. It is important to remember:

- separation and guarding with ground pins in component interface reduces power to signal coupling, thus reducing connector count.
- if a dedicated grounding system is a factor in construction standard 2-sided boards can be used in the design of printed wiring boards.
- to produce a ground plane that minimizes coupling, add ground jumpers and landfill to standard two-sided boards.
- harness design coupling can be estimated prior to detail design and separation; shielding or coax cable can alleviate common class EMI coupling problems.
- wire wrap boards handling T^2L and Schottky signals should always use a ground plane; location of long runs to the first wire wrap level and the addition of a third level ground grid reduces coupling and risetime ringing effects.

This article was reprinted with permission from a paper presented by G.P. Condon and J.S. Thompson, EMC Engineering, General Electric, Space Systems Division, Valley Forge, PA, at the Delaware Valley Chapter Meeting of the Electronic Connector Study Group, November 1980.