Synchronised disturbance pulses at the module level

Fault localisation and remedy in an application that has failed a compliance test can be a real challenge, particularly with highly integrated modules. Looking for the causes becomes even more difficult if several fault patterns occur in one and the same test.
Suitable measurement tools can make it much easier for the developer to locate faults and find the causes faster.

The present case relates to the control unit of a disturbance generator that is being developed.
The module consists of a 2-layer circuit board and comprises a microcontroller (TQFP), an FPGA, logic / interface modules and mechanical control elements (rotary pulse generator, pushbuttons, switches) along with the LCD display.
The entire circuit-board is close to the disturbance generator. As a result, the immunity requirements are correspondingly high.

During the compliance test according to IEC 61000-4-4 (EFT burst) the display showed erroneous output data and the interface modules crashed at a burst voltage amplitude of 800 V. Both faults occurred independently of each other.

Pulse-shaped disturbances were applied locally to different points of the module to isolate the weak point. However, the cause could not be clearly identified. Although the same disturbance was applied to the module, the described fault pattern only occurred at irregular intervals. Apart from local weak points, the time (relative to the controller's program sequence) seemed to play a decisive role.

The disturbances hence had to be applied to the module at defined intervals to allow a more precise analysis.
First of all, an appropriate way had to be found to couple the disturbances locally into the module at a precise time. The following figure shows a schematic diagram of the test set-up that was finally chosen:

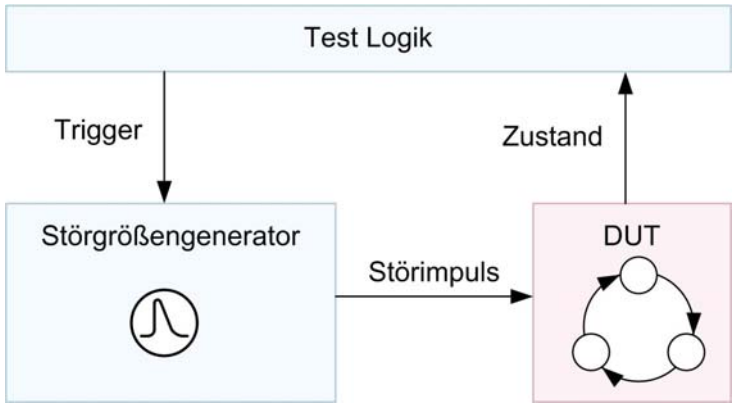

Figure 1 – Block diagram of the test set-up

The entire test set-up consists of three components:

1. Device under test (DUT)
2. Disturbance generator
3. Test logics.

The test logics determines the precise time when the disturbance pulse is applied to the device under test. Based on the controller's program state, it generates a trigger signal for the disturbance generator in the device under test. The disturbance generator in turn generates a disturbance pulse which can be coupled into different circuit components of the device under test.
This means that faulty functions can be assigned to not only pins or lines but also to the specific points in the firmware of the device under test.

Level shifters in conjunction with an FPGA make up the test logics and allow flexible trigger conditions. The requirements for the disturbance generator were initially defined to find a suitable device for this test set-up:

- possibility of applying disturbances selectively to individual lines and/or pins

- capacitive / inductive coupling of the disturbances
  (conducted coupling makes it more difficult to apply the disturbance to several different points in the device under test)

- magnetic field as the inductive disturbance coupling mechanism
  (a disturbance which is coupled in via an electric field is too small due to its low coupling capacitance)

- the disturbance has to be coupled into a selected line at a predefined time

- the disturbance's pulse shape need not comply with a certain standard but must satisfy two prerequisites:
  - rise time of the disturbance pulse edge ≤5 ns
  - the generated pulse shape should remain the same (with a max. allowance of 10% for repetitions)

- the disturbance generator must react quickly before the controller changes over to the next state
  - the microcontroller is clocked at 70 MHz → this results in a trigger-to-disturbance pulse delay of <14 µs

Only an ESD pistol, an EFT/B generator and a MINI burst generator were initially considered as potential disturbance generators. The aforementioned requirements meant that an ESD pistol could not be used since it did not allow any selective coupling into individual lines. The MINI burst generator was also ruled out since it did not permit external triggering.

The EFT/B generator initially seemed to meet all of the required criteria. The trigger-to-disturbance pulse delay still had to be determined. The trigger input of the EFT/B generator was connected to a function generator for this purpose. Both the trigger and the output of the EFT/B generator were connected to an oscilloscope. The following figure shows the result of this measurement:

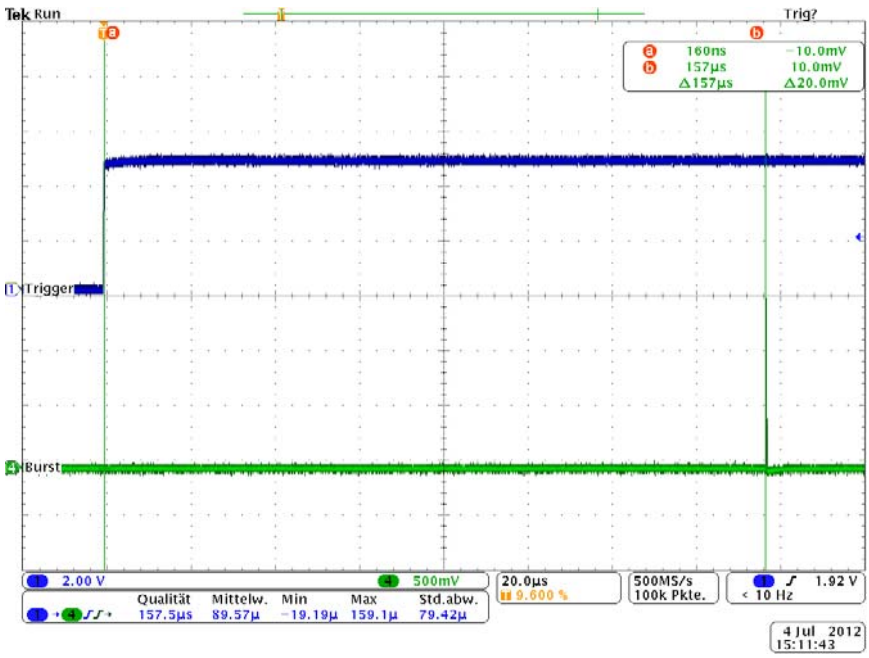

Figure 2 - Trigger-to-pulse delay of the EFT/B generator

A pulse was not generated on the output of the EFT/B generator until 157 µs after triggering by the function generator. This response time of the EFT/B generator was too long for the task that we wanted to perform. Apart from the long delay, another problem was to introduce the disturbance pulse into the device under test with as little bias as possible and without any negative effect on its edge steepness. This could not be guaranteed with the test set-up.
The test task described could not be performed with the existing technical equipment. A new test means was thus designed.

The aforementioned battery-operated MINI burst generator was used as a basis for the new equipment. The pulse provided by the disturbance generator was shaped close to the coupling electrode (distance of around 3 cm) so that the pulse shape was not significantly affected.
A test showed that the interference effect on individual lines of the device under test was also strong enough to cause faults. One problem here was that there was no triggering. The generator (including its internal power supply) was activated via a simple ON / OFF switch in the existing version. This resulted in a start-up time in the time range of several milliseconds. Replacing the mechanical with an electronic switch could not solve the problem. All circuit parts except the pulse shaper were modified instead.

The following figure shows a schematic diagram of the disturbance generator as well as the disturbance coupling mechanism.

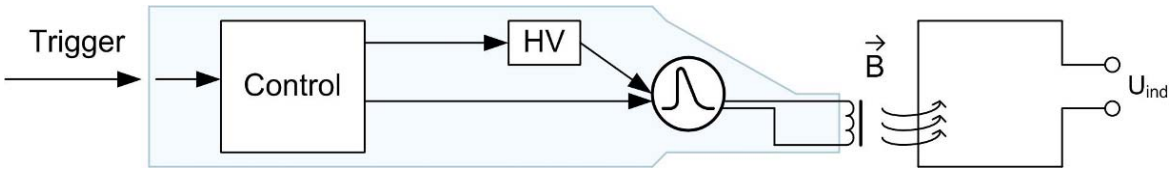

Figure 3 - Modified MINI burst generator

The internal high-voltage generation was made to work constantly by converting the generator circuit to mains operation. A control logics now controlled the pulse generation and ensured a consistent pulse shape at all trigger frequencies up to 5 kHz.
The housing requirements led to a lack of space and prevented the integration of a powerful high-voltage supply. This entailed a decrease in the amplitude of the disturbance pulse as of a pulse repetition frequency of > 5 kHz. The amplitude, however, still corresponded to 90 % of the maximum disturbance voltage that can be achieved at 10 kHz.

Initial measurements on the MINI burst generator that was modified as described above showed that the defined requirements can be met:

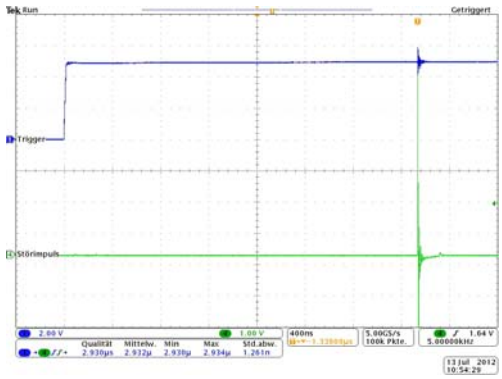
Figure 4 – Trigger-to-pulse delay of the MINI burst generator

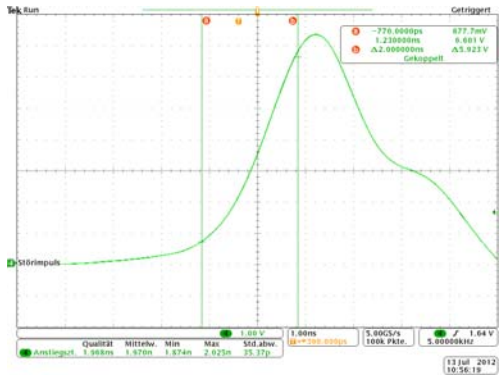
Figure 5 – Disturbance pulse shape of the MINI burst generator

The trigger-to-pulse delay was 3 µs at a jitter of <100 ns. This meant that there were sufficient reserves to time the disturbance pulses. The consistent disturbance pulse shape with an edge steepness of approx. 2 ns also complied with the required parameters.

The test procedure was as described below:
The current state of the controller was output to the test logics which generated a trigger pulse for the disturbance generator depending on the configuration. Each trigger pulse caused a disturbance pulse. These disturbance pulses could then be applied to different points in the application. After the module had been examined for potential weak points, the next controller state was used for triggering via the test logics.

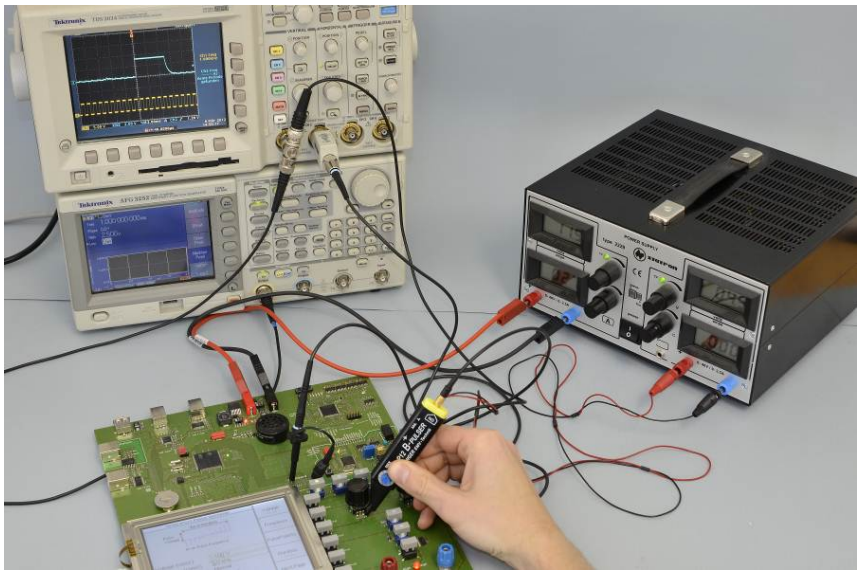

Figure 6 – Test set-up (optional)

The described fault patterns could be reproduced using the test set-up shown in Fig. 6. The disturbance was applied to the address / data lines at the time of the data acceptance. The new test generator did not affect any other circuit components.
The module's immunity increased several times over after 1 K resistors had been soldered in the address line to reduce the disturbance current as a counter-measure. Our work was well worth the effort. The time and cost required to develop a new test generator paid off in the form of a robust circuit which can be accommodated in a plastic housing and needs only little shielding. Thanks to this EMC reserve, the new product will have a longer technical service life on the market.

Test Logik	Test logics
Störgrößengenerator	Disturbance generator
Störimpuls	Disturbance pulse
Zustand	State

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