Estimation of power/ground-reference plane decoupling noise in multi-layer PC boards

A simple method accurately estimates the noise from ICs to boost engineering accuracy.

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DECOUPLING POWER AND GROUND-REFERENCE planes is probably one of the most misunderstood design areas and certainly gives rise to the most myths about the "correct" decoupling strategy. The use of decoupling capacitors connected between the power and ground-reference planes on a printed circuit board (PCB) is a common practice to help ensure proper functionality and to reduce EMI emissions from printed circuit boards. The optimum number of decoupling capacitors—and the optimum value of those decoupling capacitors—remains a topic of debate between EMC engineers and design engineers. Some typical rules-of-thumb require a decoupling capacitor for each power pin on an IC. Other rules-of-thumb require at least one decoupling capacitor per side of physically large ICs. Still other rules-of-thumb require decoupling capacitors spread evenly over every square inch of the board. Very little real information about the optimum approach is available in the technical literature. These rules of thumb often result in a drastic overdesign of the decoupling strategy since the saying "better safe than sorry" is usually applied. Many of these so-called rules-of-thumb are in reality based on myth. Moreover, outright myths exist and are published, further confusing the general design community. Some of these myths are based on some rationale to justify them; others are not. One recent myth claimed that the decoupling capacitors actually caused the emissions! However, most myths are not so easy to discount.

Traditionally, the chosen values of the decoupling capacitors are based largely upon habit and the experience of the EMC engineer. Values of 0.01 µF or 0.1 µF are typically used. Often, smaller capacitors are used in parallel with the main decoupling capacitor to provide a high frequency and a low frequency filtering effect. However, potential cross resonances can have a negative effect when using multiple capacitors in close proximity. In short, the design and analysis of the power plane decoupling (between a power plane and a ground reference plane) has been historically difficult. With on-board clock speeds of 400 to 800 MHz becoming common, a more rational approach must be taken to optimize the design of decoupling capacitors on the printed circuit board.

There have been a number of papers analyzing the noise transfer from an IC source at one location on the board to another location on the board. Other papers have analyzed the impedance at a given location on the board. However, all of these papers either have given no in-